Chapter 5 Multiplexer and demultiplexer

5-1 Practice purpose

1. To understand digit multiplexer's theory and function
2. To understand digit demultiplexer's theory and function

5-2 Practice theory

A multiplexer (data selector)(MUX) connects input line to single output line and de-multiplexer (data dispatcher)(DEMUX) is the opposite, which connects one input line to one of the many output lines. This chapter is mainly to discuss and practice these two electronic circuits.

5-2-1

Multiplexer or data selector can choose many data inputs and only input one of them to output logic electronic circuit. The procedure to input data to the output end is controlled by select input. (Sometimes it is called address input). Figure 5-1 is the symbol of MUX. In this figure, the big arrow shows input and output with one or more lines.
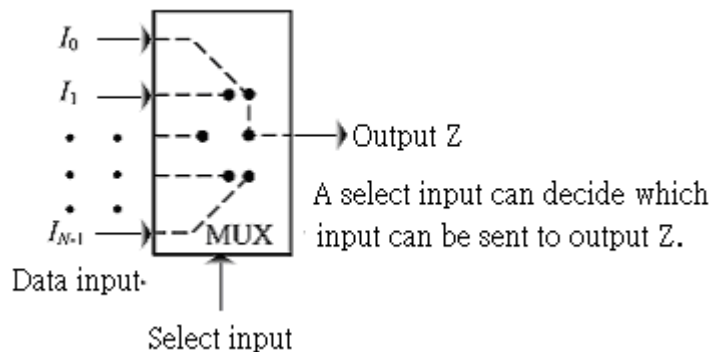

Figure 5-1 MUX symbols

The function of MUX is like a digital control multi positions switch *. It means that select input's digit numbers can control the switch. The data input can be sent to output. For example, for certain selected inputs, input Z is like input I_0, but to other selected inputs, Z is like I_1, vice verse. In other words, MUX chooses one input from N inputs and sends it to the signal output and this is called multiplexing.

Basic two input multiplexers

Figure 5-2 shows data input I_0 and I_1 and select input S's two input MUX logic electronic circuit. We can decide which logic circuit to add to S input, which AND gate can be stimulated, and input data to output Z through OR gate. We can see the output formula is as:

$$Z = I_0\overline{S} + I_1S$$
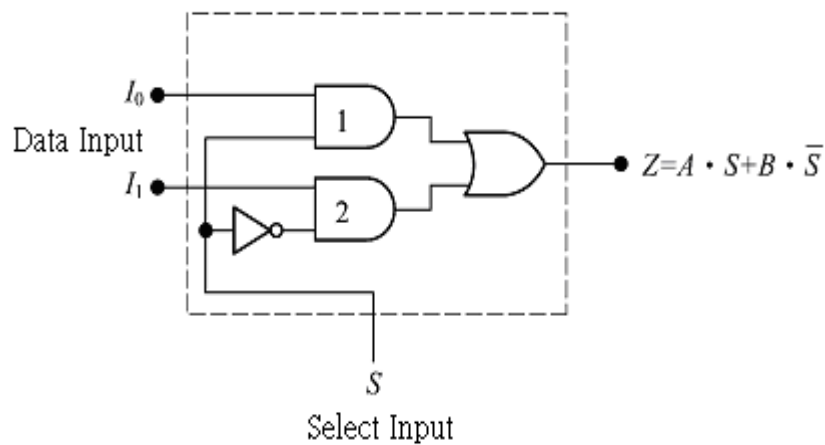
$$S = 0 \quad \text{so}$$

$$Z = I_0 \cdot 1 + I_1 \cdot 0$$

$$= I_0$$

It means that Z has the input signal I_0, and I_0 can be a set logic circuit or spontaneous logic signal. S=1, so:

$$Z = I_0 \cdot 0 + I_1 \cdot 1 = I_1$$

It means z has input signal I_1.

S	Input
0	$Z = I_0$
1	$Z = I_1$

Figure 5-2 Two MUX

Four input MUX

As figure 5-3 shows, four input MUX is based on the same theory. It has four inputs and according to S_1, S_0 select input four possible combinations to send four input choices to outputs. Each data input is combined with different select input circuit combination gate, I_0 and S_1S_2. When gates combine together, output I_0 to Z through AND gate when S1=0, S0=0. The table shows the three input select codes' outputs.

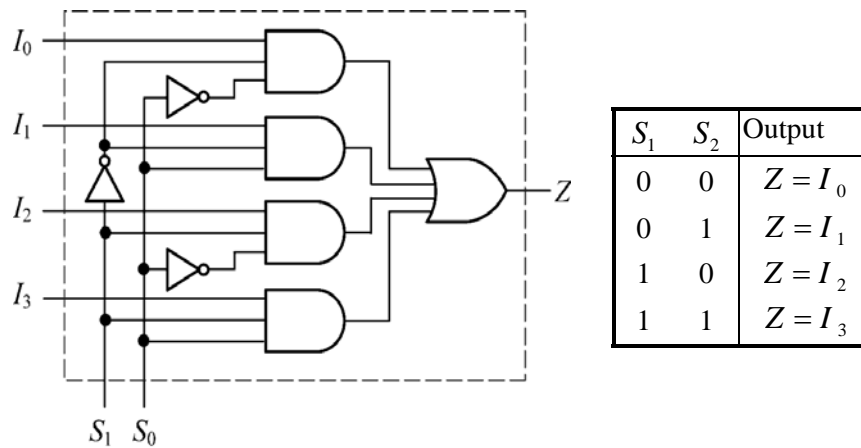| S_1	S_2	Output
0	0	$Z = I_0$
0	1	$Z = I_1$
1	0	$Z = I_2$
1	1	$Z = I_3$

Figure 5-3 Four input MUX

5-2-2 De-multiplexer

Multiplexer can receive many inputs and send one to output. De-multiplexer, also called data dispatcher, only receives a single signal and dispatches to many outputs, which is opposite to multiplexer. Figure 5-4 is DEMUX figure, the big arrow represents one or many lines and the selected input code decides which data input goes to which outputs. In other words, DEMUX takes one input and dispatches it to N output through a multi position switch.
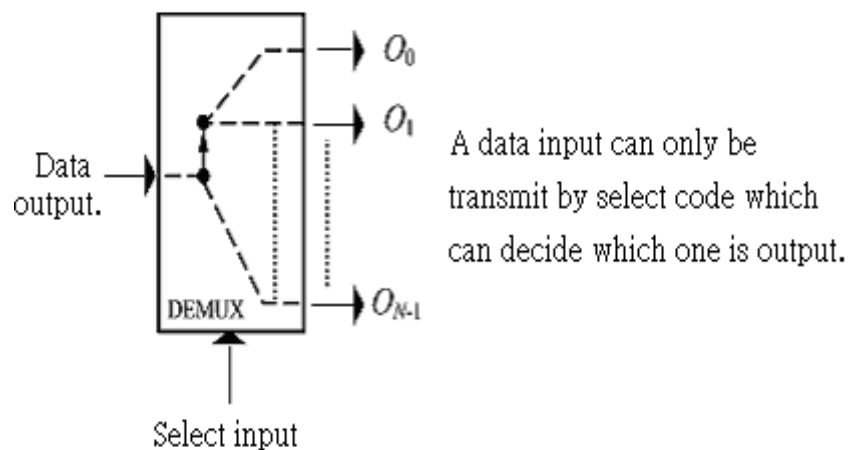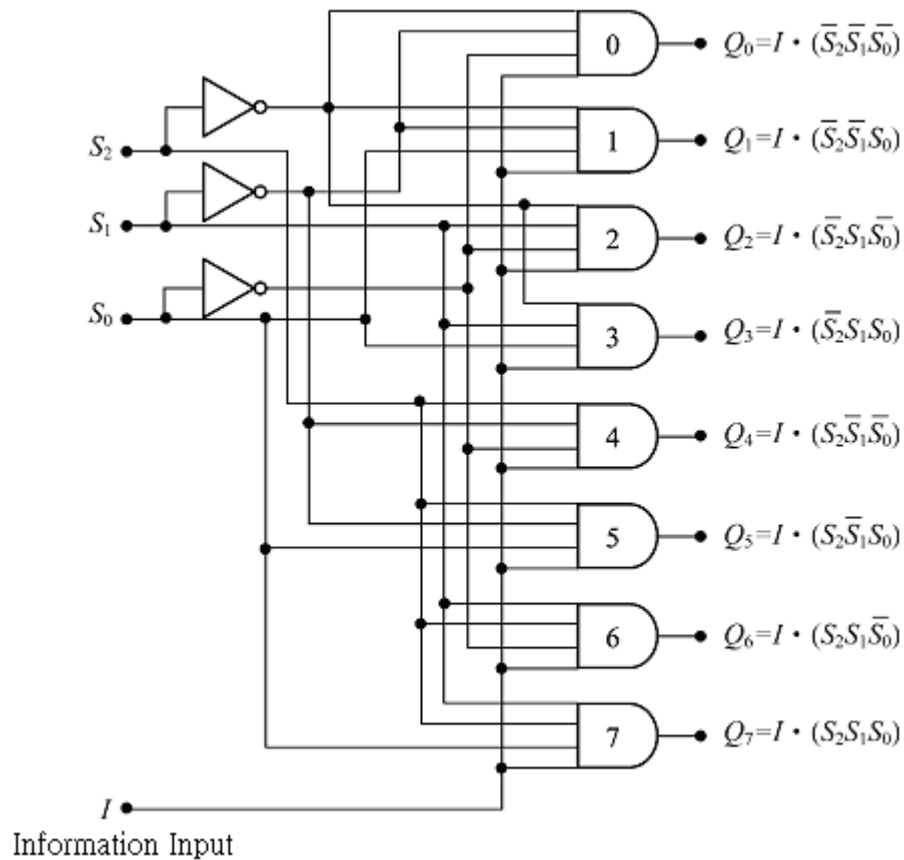

A data input can only be transmit by select code which can decide which one is output.

Figure 5-4 DEMUX

$$Q_0 = I \cdot (\bar{S_2}\bar{S_1}\bar{S_0})$$

$$Q_1 = I \cdot (\bar{S_2}\bar{S_1}S_0)$$

$$Q_2 = I \cdot (\bar{S_2}S_1\bar{S_0})$$

$$Q_3 = I \cdot (\bar{S_2}S_1 S_0)$$

$$Q_4 = I \cdot (S_2\bar{S_1}\bar{S_0})$$

$$Q_5 = I \cdot (S_2\bar{S_1}S_0)$$

$$Q_6 = I \cdot (S_2 S_1\bar{S_0})$$

$$Q_7 = I \cdot (S_2 S_1 S_0)$$

Select Code			Output							
S_2	S_1	S_0	O_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Figure 5-5 1 to 8 lines DEMUX

Figure 5-5 is 1-8 lines DEMUX. Single data input line I is connected to all eight AND gates, but only one of AND gates can be chosen. For example, $S_2 S_1 S_0 = 000$, only AND gate 0 is stimulated and the data input I is presented output O_0. Its chosen code can send input I to other outputs. The truth table explains it.

5-3 Practice items

5-3-1

Experiment steps

1. 2 to 1 MUX circuit as figure 5-6
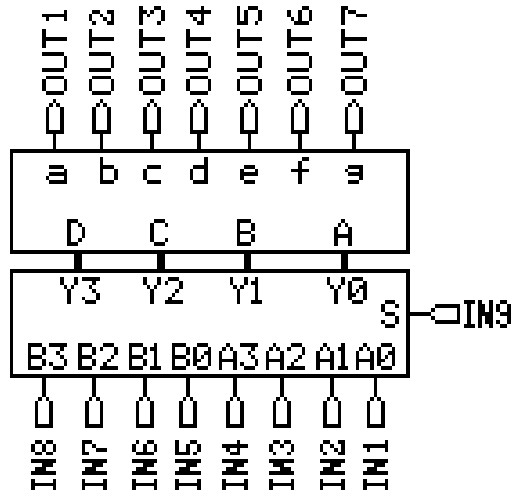

Figure 5-6

2. Input: Connect CON7 S1 to CON1 IN1
              Connect CON7 S2 to CON1 IN2
              Connect CON7 S3 to CON1 IN3
              Connect CON7 S4 to CON1 IN4
              Connect CON7 S5 to CON1 IN5
              Connect CON7 S6 to CON1 IN6
              Connect CON7 S7 to CON1 IN7
              Connect CON7 S8 to CON1 IN8
              Connect CON6 S9 to CON1 IN9

Output: Connect CON4 OUT1 to 7- SEGMENT CON10 L1 a
              Connect CON4 OUT2 to 7-SEGMENT CON10 L1 b
              Connect CON4 OUT3 to 7- SEGMENT CON10 L1 c
              Connect CON4 OUT4 to 7-SEGMENT CON10 L1 d
              Connect CON4 OUT5 to 7- SEGMENT CON10 L1 e
              Connect CON4 OUT6 to 7-SEGMENT CON10 L1 f
              Connect CON4 OUT7 to 7- SEGMENT CON10 L1 g

3. Switch S1-S9 after finished connecting, as table 5-1. 0 means low logic, LED off. 1 means high logic, LED on.

4. Record 7-segment changes in table 5-1.

S (S9)	A_3 A_2 A_1 A_0 (S4) (S3) (S2) (S1)	B_3 B_2 B_1 B_0 (S8) (S7) (S6) (S5)	Y_3 Y_2 Y_1 Y_0 Result
0	0 0 0 1	0 0 1 0	
0	0 0 1 1	0 1 0 0	
0	0 1 0 1	0 1 1 0	
1	0 0 0 1	0 0 1 0	
1	0 0 1 1	0 1 0 0	
1	0 1 0 1	0 1 1 0	

Table 5-1

5. From table 5-1, we know when S   0, Y   ___(A or B), when S   1, Y   __(A or B).

5-3-2

Experiment steps

1. 4 to 1 MUX circuit as figure 5-7
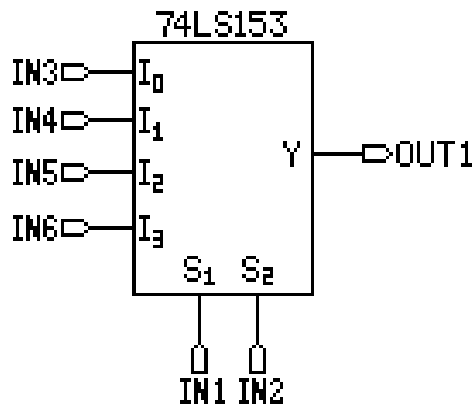

Figure 5-7

2. Input: Connect CON7 S1 to CON1 IN1
             Connect CON7 S2 to CON1 IN2
             Connect CON7 S3 to CON1 IN3
             Connect CON7 S4 to CON1 IN4
             Connect CON7 S5 to CON1 IN5
             Connect CON7 S6 to CON1 IN6
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q9
2. Switch S1-S6 after finished connecting, as table 5-2. 0 means low logic, LED off.
    1 means high logic, LED on.
3. Record LED changes in table 5-2.

SOP	IN3 (S3)	IN4 (S4)	IN5 (S5)	IN6 (S6)	IN1 (S1)	IN2 (S2)	OUT1 (Q9)
0	0	0	0	0	0	0	
1	0	0	0	1	0	1	
2	0	0	1	0	1	0	
3	0	0	1	1	1	1	
4	0	1	0	0	0	0	
5	0	1	0	1	0	1	
6	0	1	1	0	1	0	
7	0	1	1	1	1	1	
8	1	0	0	0	0	0	
9	1	0	0	1	0	1	
10	1	0	1	0	1	0	
11	1	0	1	1	1	1	
12	1	1	0	0	0	0	
13	1	1	0	1	0	1	
14	1	1	1	0	1	0	
15	1	1	1	1	1	1	

Table 5-2

5-3-3 1 to 4 DMUX

Experiment steps

1. 1 to 4 DMUX circuit as figure 5-8 connecting the circuit properly.
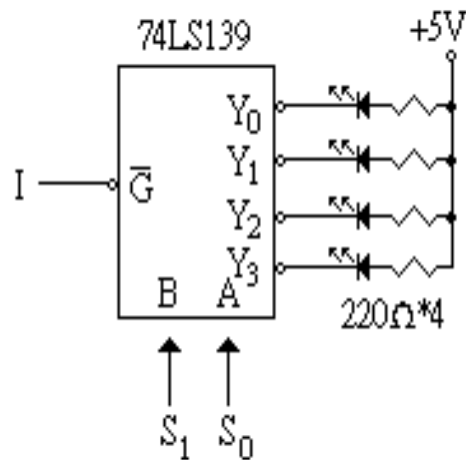

Figure 5-8 1 to 4 DUMX circuit

2. Input: Connect CON7 S1 to CON1 IN1
             Connect CON7 S2 to CON1 IN2
             Connect CON7 S3 to CON1 IN3
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q9
             Connect CON4 OUT2 to LED DISPLAY CON15 Q10
             Connect CON4 OUT3 to LED DISPLAY CON15 Q11
             Connect CON4 OUT4 to LED DISPLAY CON15 Q12
3.Record LED changes in table 5-3, when LED is on, Y=0, when LED is off, Y=1.

Input			Output			
I	S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	0				
1	0	0				
0	0	1				
1	0	1				
0	1	0				
1	1	0				
0	1	1				
1	1	1				

Table 5-3 Truth table

4. From table 5-3, we know when $S_1S_0=00$, $Y_0Y_1Y_2Y_3=$____, when $S_1S_0=01$, $Y_0Y_1Y_2Y_3=$____ when $S_1S_0=10$, $Y_0Y_1Y_2Y_3=$____, when $S_1S_0=11$, $Y_0Y_1Y_2Y_3=$____.

5-4 Questions and Discussion

1. What decides the input of MUX output?
2. Assume there is a 32 input lines MUX, then what is the logic input?
3. By using 8 of 1 data selector/MUX design to match the following logic function circuit.

$$\overline{E} = \overline{A} \cdot \overline{B} \cdot C \cdot D + A \cdot B \cdot \overline{C} + A \cdot B \cdot \overline{D}$$