Chapter 8 Shift Register Practice

8-1 Practice purpose

1. To understand the shift register's theory and appliance

8-2 Practice theory

A register usually saves data or makes data shift. When it shifts data the movement is called a shift register. In general, a single flip-flop can save multi information, therefore, n digit register needs n flip-flops. This kind of register, among much of the digital system, is used as temporary data, which is why it is call a register.
There are usually only two kinds of data, serial or parallel. Serial data is sent by single line and made by binary system with time orders. Parallel data is a preset digit and when it moves, all the digit information moves as well and there is no time order. Register's shift allows the saved data to move from one to the other, or move in and out. There are two kinds of shifts:

1. Serial shift left and right
2. Parallel shift in and out

According to the combination of two information shifts, there are four forms of general shift registers:

1. Serial in, serial out (SISO) such as 7491.
2. Serial in, parallel out (SIPO) such as 74164.
3. Parallel in, parallel out (PIPO) such as 74178, 74179.
4. Parallel in, serial out (PISO) such as 74165, 74166.

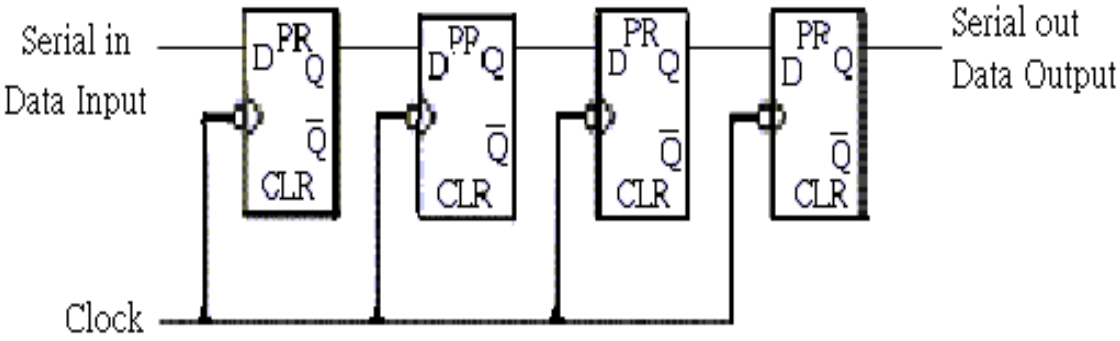
Of course some shift registers have all the above functions, and they are called bidirectional universal shift registers.

Table 8-1 common shift register

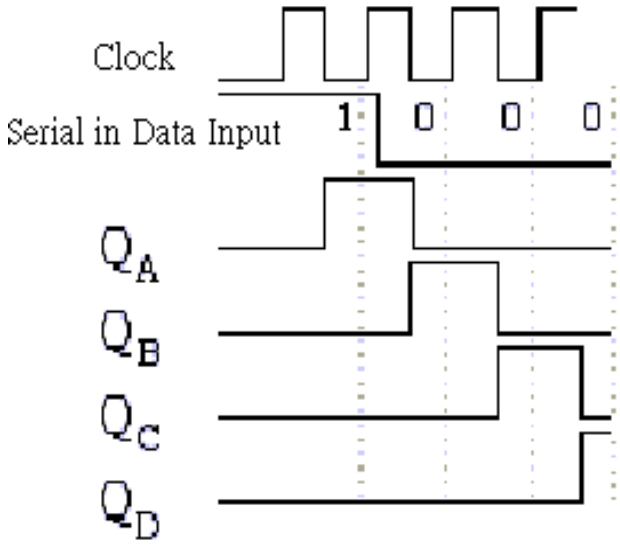
Function	Data bit	Element
SISO	8	7491,74164,74165
SIPO	8	74164
PIPO	4	7494
	8	74165,74166
PISO	4	7495,74178,74195
	8	74198,74199

8-2-1 Serial in Serial Out: SISO

Figure 8-1 (a) four bit SISO shift registers. Data is serial into D end. In each clock's negative edge, data shift one bit to the right and after four timer clock periods, data is serial out from the very right flip-flop.



(a) Circuit

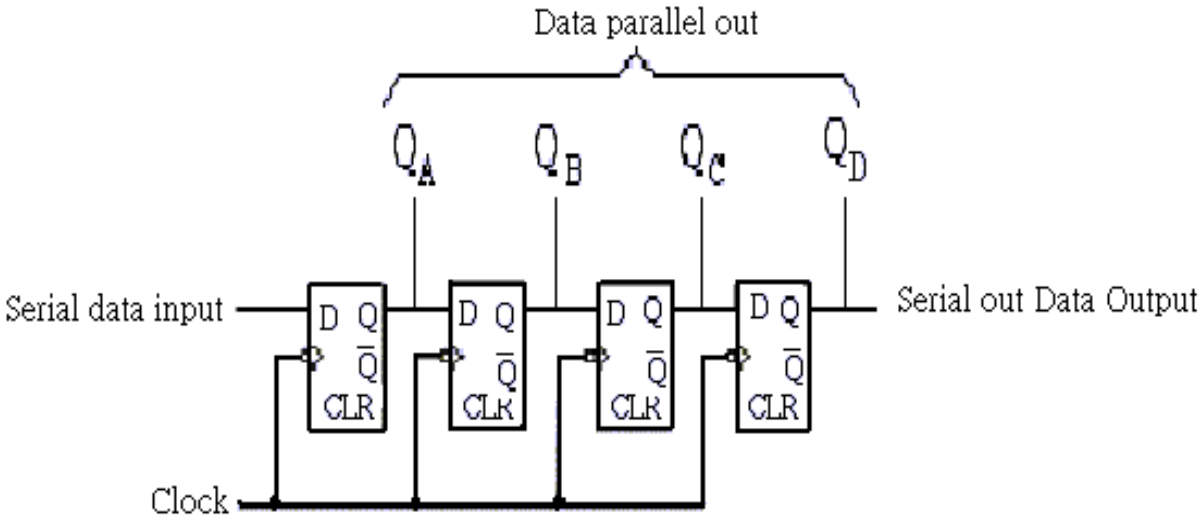


(b) SI 1000B

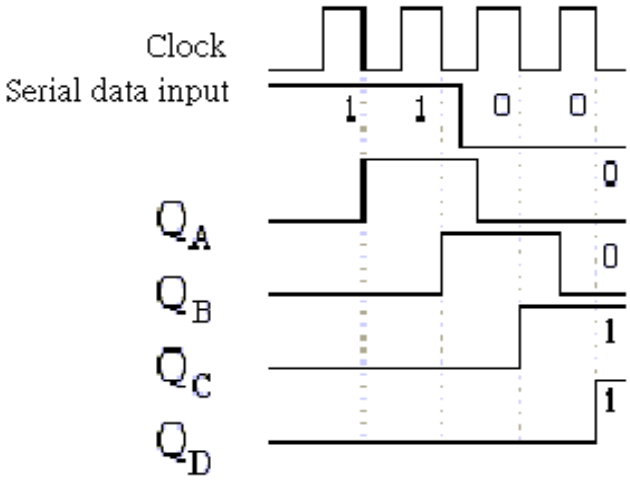
Figure 8-1 4bit SISO shift register

8-2-2 Serial In-parallel Out: SIPO

As figure 8-2, 4 bit SIPO. Data is serial in to D end. In each clock's negative edge, data shift one bit to the right and after four timer clock periods, 4 bit data is parallel out from 4 flip-flops' output ends.



(a) Circuit

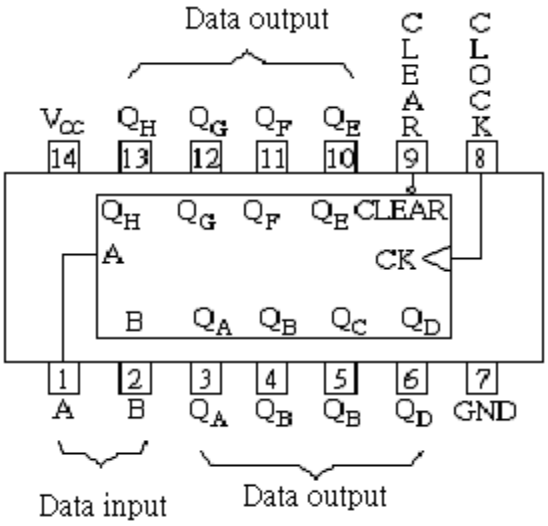


(b) SI 100B

Figure 8-2 4 bit SIPO shift register

74164 IC

74164 IC is 8 bit PISO register, as figure 8-3. 741644 has two parallel input ends, A and B. Assume data is input from A and B is the control line, so when B=0, NAND gate is stopped. Meanwhile S=0, R=1, when each clock negative edge changes, the data 0 is shifted to flip-flop, after 8 clocks, the register's content all turn to 0. When B=1 NAND is stopped and at the same time, the parallel is shifted to the register. Also, if the data is output by Q_H, then 74164 is as PIPO shift register.



(a) 74164 pin figure

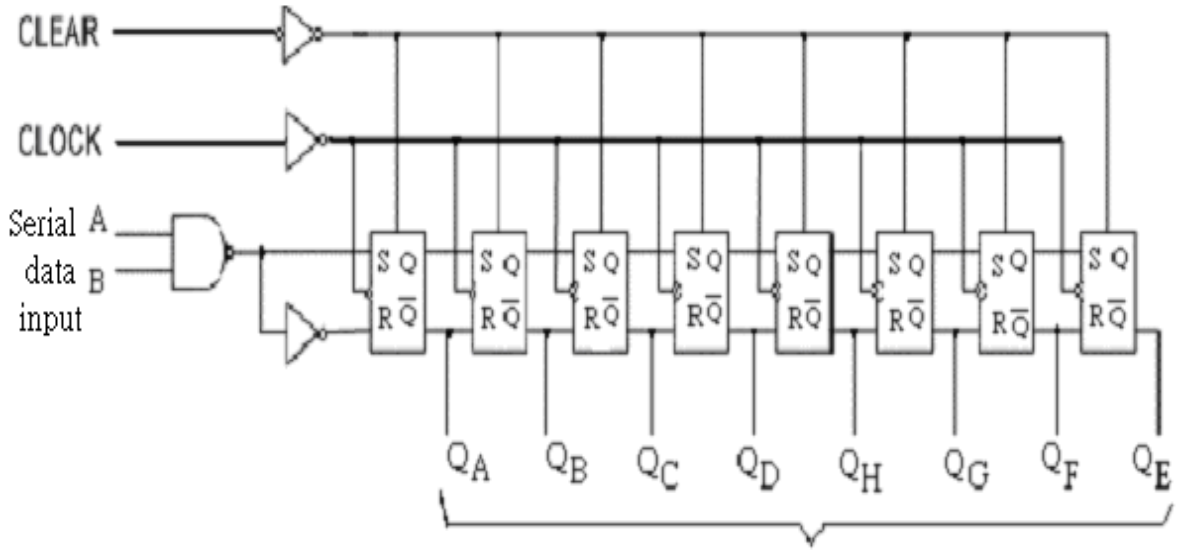
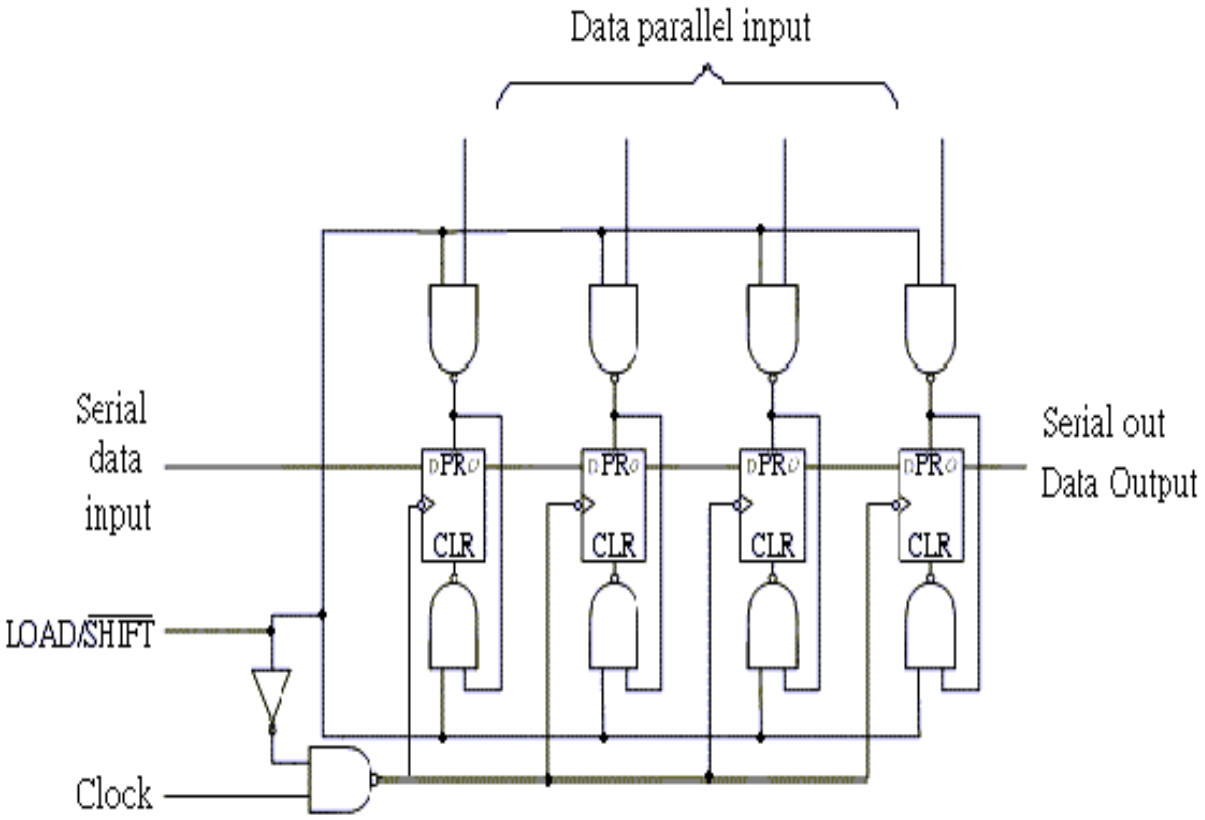


Figure 8-3 74164 8 bit shift register

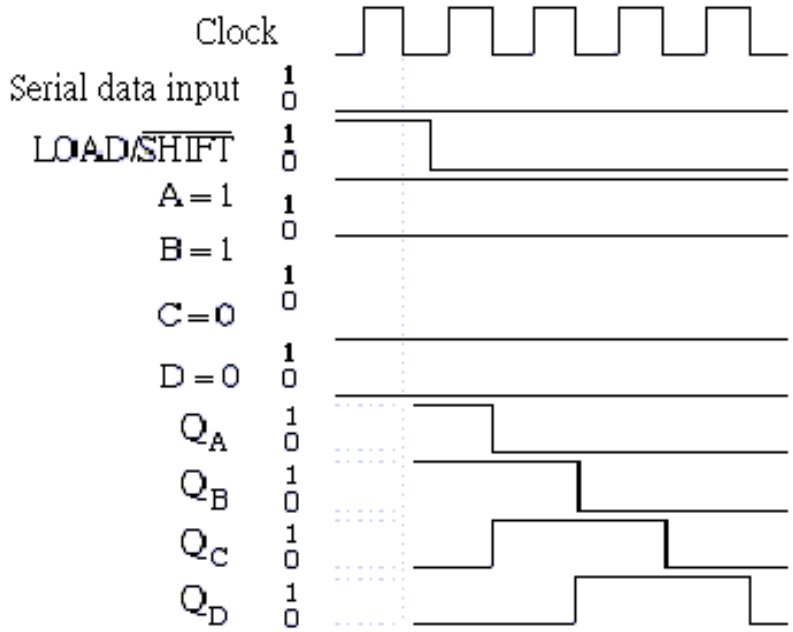
8-2-3 Parallel in Serial Out: PISO

As figure 8-4, 4 bit PISO shift register. When LOAD/$\overline{SHIFT}$ control data's LOAD or SHIFT movements. When LOAD/SHIFT =1, clock is stopped and the received data, at this time, parallel data is loaded to flip-flop. $Q_A Q_B Q_C Q_D = ABCD$.

When LOAD/$\overline{SHIFT}$ = 0, the clock is stopped and parallel data is stopped as well. The data at each clock negative edge flip-flop shifts to the right for one bit and follows the order of Q_D to serial out data.



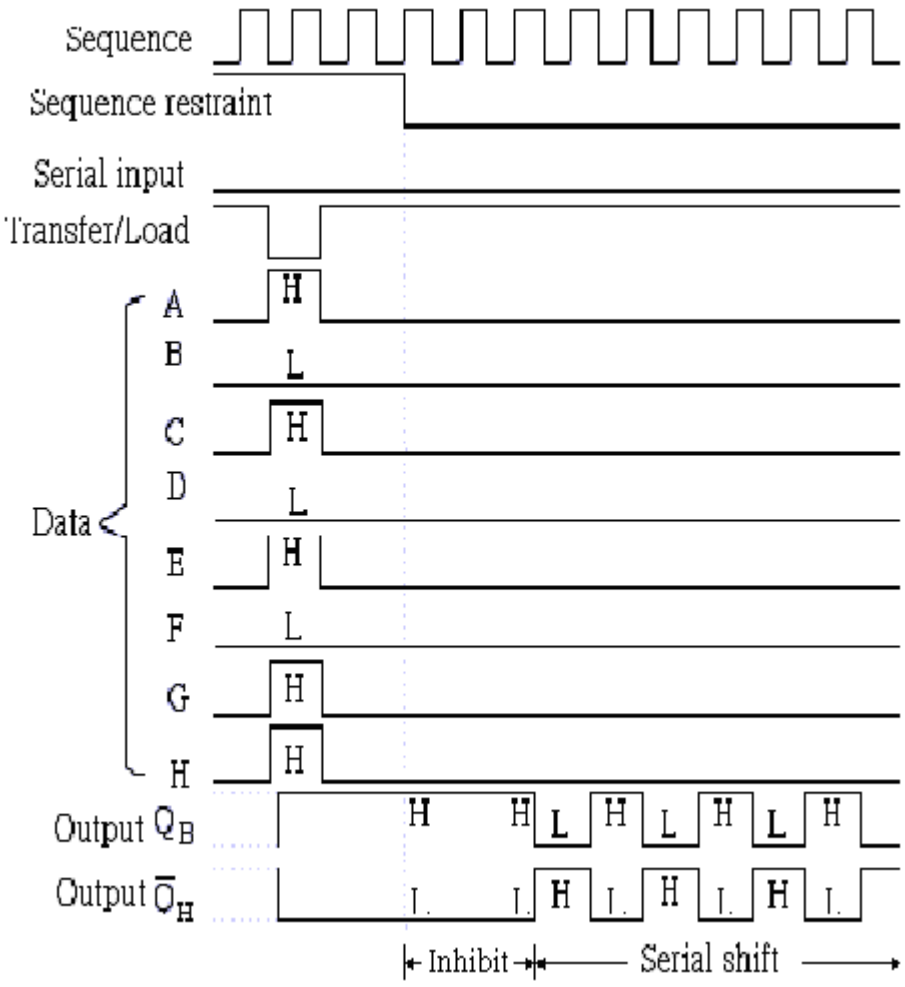
(a) Circuit



(b) SI/PO shift register

74165 IC

74165 IC is 8 BIT SO shift register. As figure 8-5, the data input is controlled by SHIFT/$\overline{\text{LOAD}}$, when SHIFT/$\overline{\text{LOAD}}$ = 0, data is parallel into input end, when SHIFT/$\overline{\text{LOAD}}$ = 1, and CK INHIBIT= 0, data is shifted in from serial in.



(b) Times figure

Figure 8-5 74165 6 bit shift register

8-2-4 Parallel in Parallel Out: PIPO

As Figure 8-6, 4 bit PIPO shift register. At a clock negative edge and parallel data and also load to flip-flop. Keep the lock HOLD, therefore, $Q_A Q_B Q_C Q_D = ABCD$.

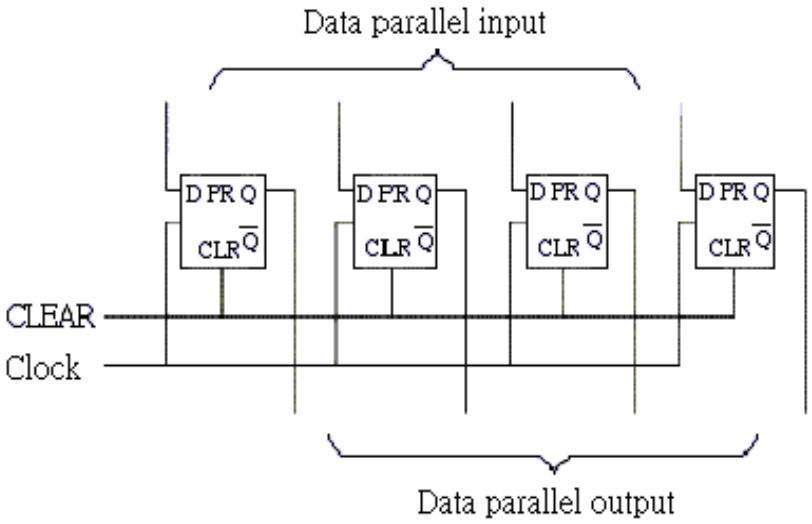


Figure 8-6 4 bit PIPO shift register

8-3 Practice items

8-3-1

Experiment steps

1. 4 bits SIPO shift Register circuit as figure8-7.

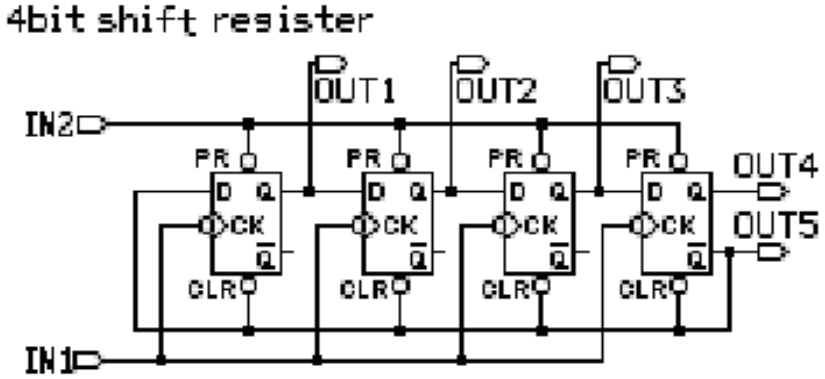


Figure 8-7

2. Input: Connect CON5 CLK 10HZ to CON1 IN1
   Connect CON7 S1 to CON1 IN2
   Connect CON4 OUT5 to CON1 IN3
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1
   Connect CON4 OUT2 to LED DISPLAY CON15 Q2
   Connect CON4 OUT3 to LED DISPLAY CON15 Q3
   Connect CON4 OUT4 to LED DISPLAY CON15 Q4
   Connect OCN4 OUT5 to LED DISPLAY CON15 Q5
3. Press S1, as table 8-2, after finished connecting. 0 means low logic, LED off. 1 means high logic, LED on.

4. Record LED changes in table 8-2.

CK	A	B	C	D	E	CK	A	B	C	D	E
	(Q1)	(Q2)	(Q3)	(Q4)	(Q5)		(Q1)	(Q2)	(Q3)	(Q4)	(Q5)
0						10					
1						11					
2						12					
3						13					
4						14					
5						15					
6						16					
7						17					
8						18					
9						19					

Table 8-2

8-3-2

Experiment steps

1. 8 bits SIPO shift Register as figure 8-8.

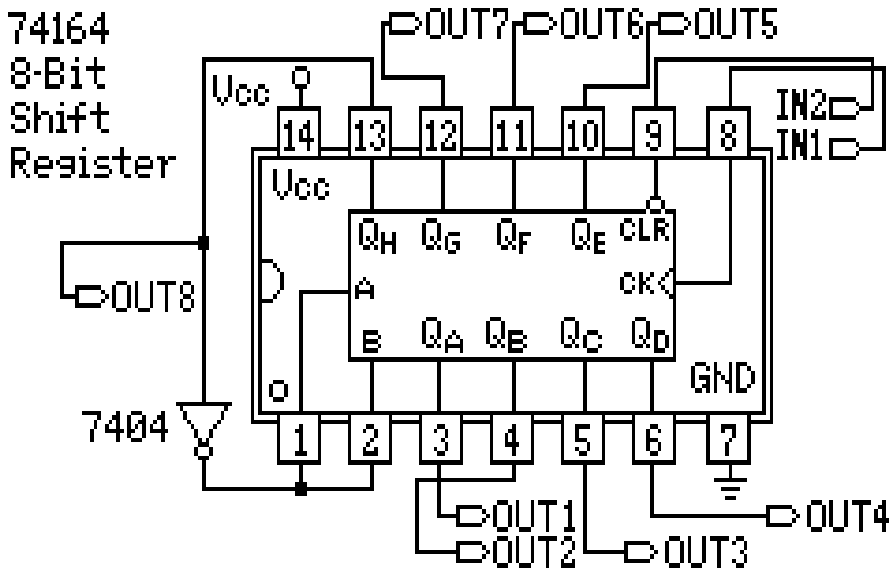


Figure 8-8

2. Input: Connect CON5 CLK 10HZ to CON1 IN1
Connect CON7 S1 to CON1 IN2
Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1
Connect CON4 OUT2 to LED DISPLAY CON15 Q2
Connect CON4 OUT3 to LED DISPLAY CON15 Q3
Connect CON4 OUT4 to LED DISPLAY CON15 Q4
Connect OCN4 OUT5 to LED DISPLAY CON15 Q5
Connect CON4 OUT6 to LED DISPLAY CON15 Q6
Connect CON4 OUT7 to LED DISPLAY CON15 Q7
Connect OCN4 OUT8 to LED DISPLAY CON15 Q8

3. Press S1, as table 8-3, after finished connecting. 0 means low logic, LED off. 1 means high logic, LED on.

4. Record LED changes in table 8-3.

CK	Q_A (Q1)	Q_B (Q2)	Q_C (Q3)	Q_D (Q4)	Q_E (Q5)	Q_F (Q6)	Q_G (Q7)	Q_H (Q8)
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
16								

Table 8-3

8-3-3

Experiment steps

1. 8 bits PISO shift Register circuit as figure 8-9.

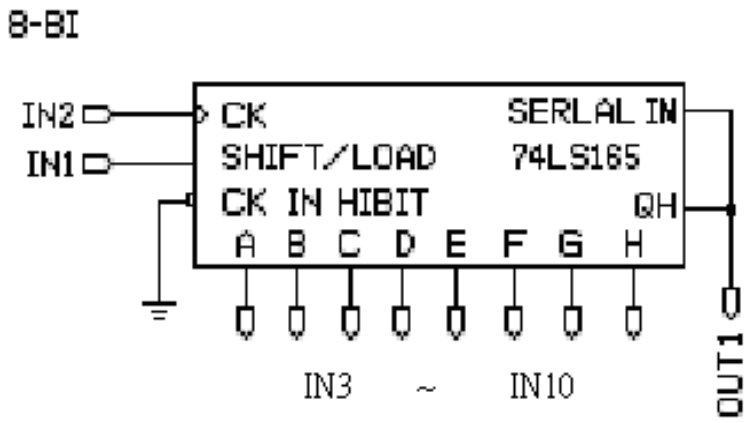


Figure 8-9

2. Input: Connect CON7 S1 to CON1 IN1
Connect CON5 CLK 10HZ to CON1 IN2
Connect CON7 S2 to CON1 IN3
Connect CON7 S3 to CON1 IN4
Connect CON7 S4 to CON1 IN5
Connect CON7 S5 to CON1 IN6
Connect CON7 S6 to CON1 IN7
Connect CON7 S7 to CON1 IN8
Connect CON7 S8 to CON1 IN9
Connect CON6 S9 to CON1 IN10
Output: Connect CON4 OUT 1 to LED DISPLAY CON15 Q1
3. Set up PI data ABCDEFGH=11001100B and press SW to load to register.
4. Record LED changes in table 8-4 LED on means Q_H = 1 LED off, Q_H = 0.

CK	Q_H	CK	Q_H
0		5	
1		6	
2		7	
3		8	
4		9	

Table 8-4

5. Reset Parallel data ABCDEFGH=10101010B and observe LED changes.

8-4 Questions & Discussion

1. How many kinds of shift registers are there?
2. What are common shift registers?
3. How is shift register used as a calculator?