Chapter 4 Encoder & Decoder Practice

4-1 The purpose of practice to:

1. Understand the dencoder's design thesis and appliance
2. Understand the encoder's design thesis and appliance
3. Understand the display's movements.
4. Understand IC's usages.

4-2 Practice thesis

This chapter introduces the most commonly used decoder, encoder and display circuit. Under many circumstances, these functional logic circuits are made for MSI integrated circuit; usually they do not need to re-design. During the process of designing circuits, we found that the major issues are to realize
all kinds of functional circuits, choose proper MSI devices and correctly install the circuits. Of course, before designing we have to have the ability to analyze the circuits.

In general, a byte made up of n bits, which can only show maximum 2n different information, for example, a byte made by four bits can show 16 different kinds of information. (Equal to decimal system 0-15). And the circuits that can divide information from n input lines are called decoders.

There are many kinds of decoders and they all depend on what they are used for. The normal digital IC manufactured by factories is 2 lines to four line and four lines to 10 lines (BCD to decimal system), four lines to 16 lines (binary system to 16 lines), three lines to 8 lines and BCD to 7 section display decoder.

Combinational logic is circuit made by input variable, output variable and all kinds of logic device. The output status is directly showed with the input end combination. During the delivery process, it is shown with binary signals meaning 1 and 0.
The information controls logic 1 and logic 0 includes:

1. Decoding and Encoding – Transfer information's one kind of code to another code.
2. Multiplexing- Choose one output from several sources of information.
3. Demultiplexing- Dispatch information to several destinations.
4. Databusing- Transfer, by public bus, information among many devices.

The above circuits can all combine and finish with logic gate and they are called combinational logic design.

4-2-1 Decoder

Decoders transfer M outputs from N bit binary system input codes and all output lines only respond to one input combination.

Figure 6-1 is a decoder with N input and M output. Because N input can be either 0 or 1, therefore, there could be 2^N possible input combinations. For all possible input combinations, M output can only respond one active high, and the rest of them are active low. Many decoders are designed to produce active low output meaning the chosen output is active low and the rest of the output is active high. That is the reason why in the figure of decoders, there is always a small circle above output lines.

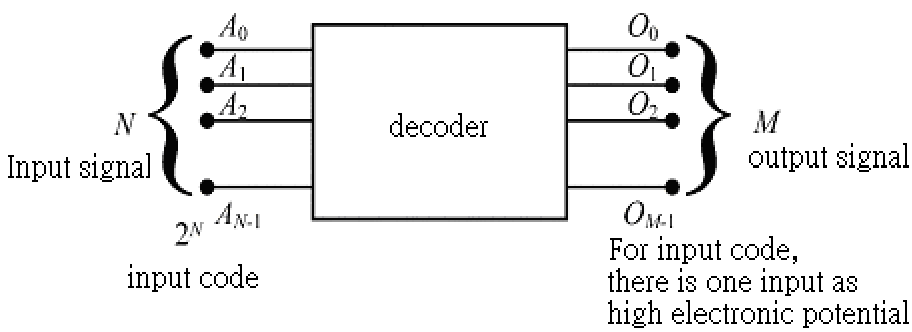
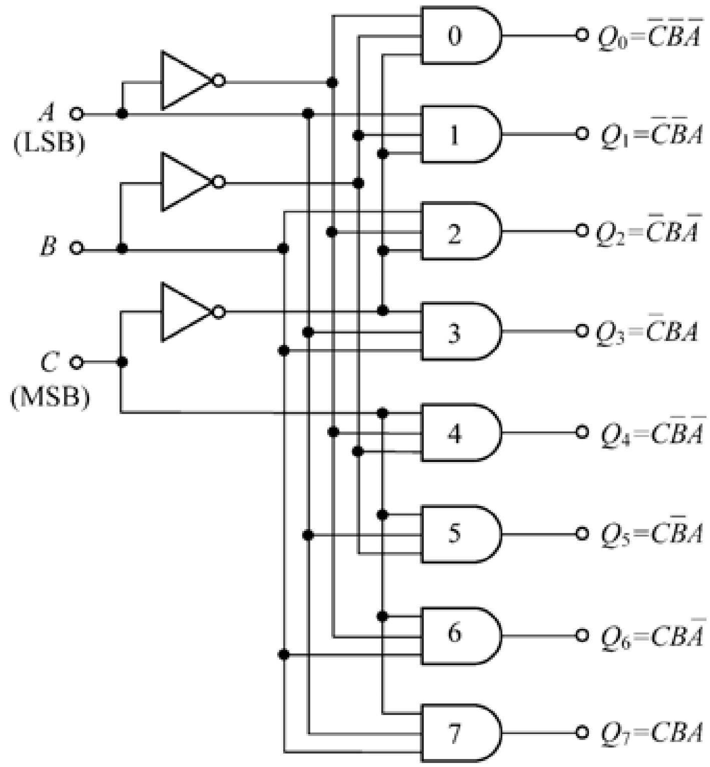


Figure 4-1 Decoder

Some decoders do not use 2^N possible input code but do use some. For example, there are four bits input codes from BCD to decimal system decoders, and there are 10 output lines responding 0000 to 1001 BCD codes. These kinds of decoders are usually designed to respond no outputs.

Figure 4-1 shows three inputs and $2^3 = 8$ output decoder. It uses AND gate and therefore the output is active high. NAND gate is used when the output is active low. Be aware that for known input codes, only binary input codes respond to equal decimal system number output (active high) (for example, output Q_6 is active high only when $CBA=110_2=6_{10})$

In fact there are many names for this kind of decoder. It can be called 3 lines to 8 lines decoder or 3-8 decoder. It is because there are three lines input and eight lines output. Furthermore, it can also be called binary to octal decoder or converter. This is because it takes 3 bits binary input codes and makes eight outputs respond to it. It can also be called 1 of 8 decoders, because only one single output responds to 8 outputs. As the figure shows, it is 3 to 8 decoder.



C B A	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0 0 0	1	0	0	0	0	0	0	0
0 0 1	0	1	0	0	0	0	0	0
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	0	0	1	0	0	0	0
1 0 0	0	0	0	0	1	0	0	0
1 0 1	0	0	0	0	0	1	0	0
1 1 0	0	0	0	0	0	0	1	0
1 1 1	0	0	0	0	0	0	0	1

Figure 4-2 3 to 8 lines decoder

Some decoders have one or more enable inputs which can control the decoder. When the enable line stays active high, then the decoder can normally function. But when the electronic potential stays active low(active low), then no matter what the input electronic potential is, all the outputs stay active low. Therefore, the decoder only responds when enable liens are active high.

4-2-2 Encoder

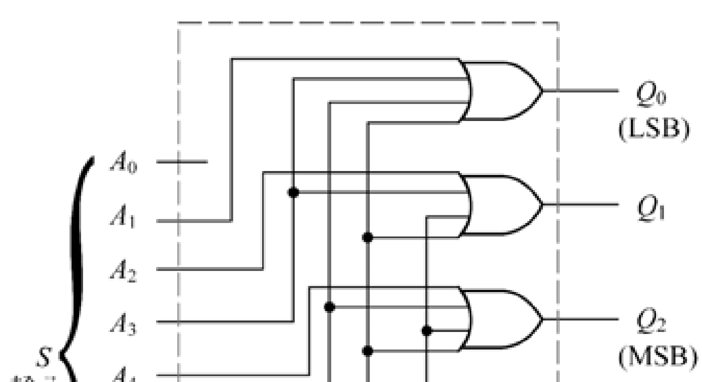
The function of encoder is totally opposite decoder’s. Encoder has some input lines and at any time there is only one line responding. Also it can produce N bit output codes. We know that Binary to octal decoder accepts 3 bits binary input codes, and one of the eight lines output lines responds. Octal to binary encoder is totally opposite, it accepts eight input lines and produces three bits binary output codes. As figure 4-3, it assumes that at some time there is only one input line as active high, there are only eight possible input situations. The circuit is designed to be A0’ *s active high, so that binary 000 is easy to output. When A1 is active high, then binary code 001 is produced. When A2 is active high, the binary 010 is produced, (see attached truth table.) The design of this circuit is very simple because it only relates to every output bit to decide the high circuit input situation which results OR. For example, the truth table shows that when input A1, A3, A5, and A7 are active high Q0 (input code LSB) must be 1, therefore we know that Q0=A1+A3+A5+A7

The rest of the output is designed in the same way. This design is only used when there are eight 2^8 possible input situations which is very simple. If at a certain time there is more than one input as active high, then the output will be wrong. If it is active high, then the output reader is 0000. Figure 4-3 encoder is called 8-3 encoder.

Switch encoder

Figure 4-4 shows how 74147 is a switch encoder. The 10 switches can be the calculator’s 0-9. These switches are open model, therefore the encoder input is normally active high, BCD output is 0000. When pressing the number, the circuit produces the number’s BCD code, because 74147 is a priority encoder therefore when pressing a number, the higher BCD code is produced.

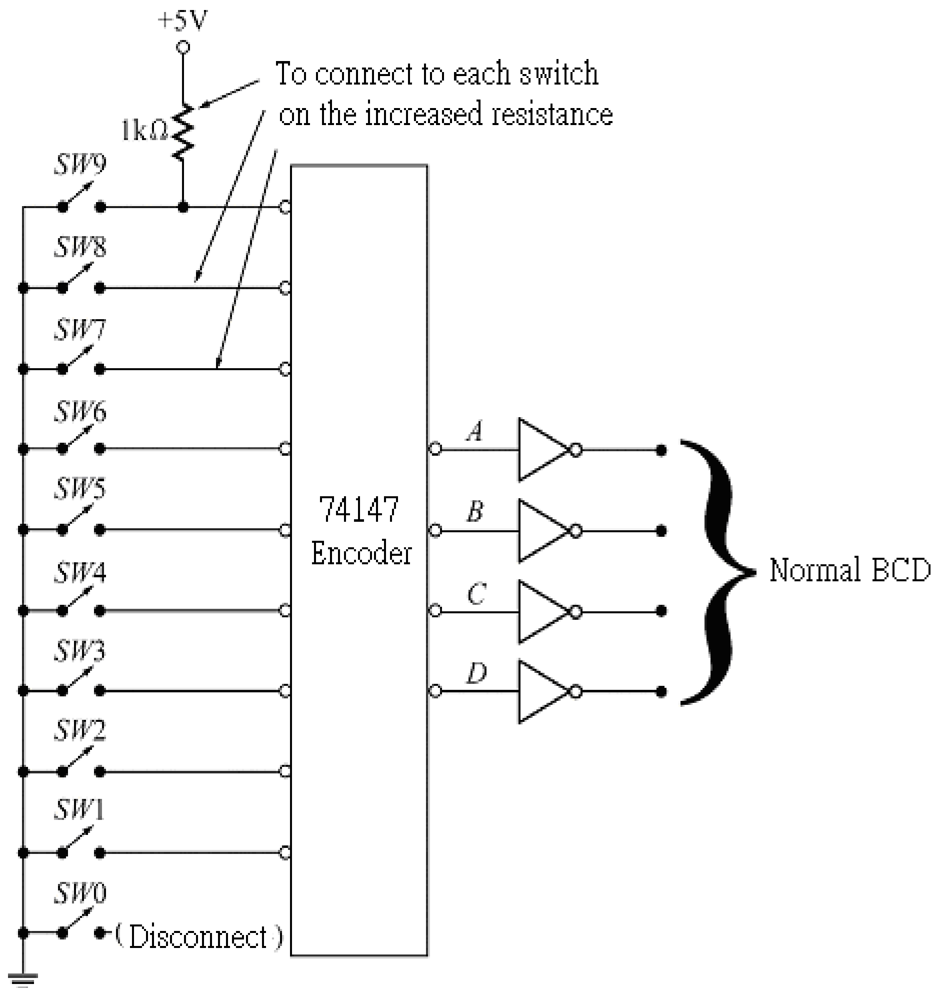
A0 is not actually connected to the circuit, because if input A1-AT are active low, then output is 000.



A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Q_2	Q_1	Q_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	0	0	1	0	0	1	0	0
0	0	0	0	0	0	1	0	1	0	1
0	0	0	0	0	0	0	1	1	1	0
(Other inputs are not allowed)								1	1	1

Figure 4-3 octal to binary encoder

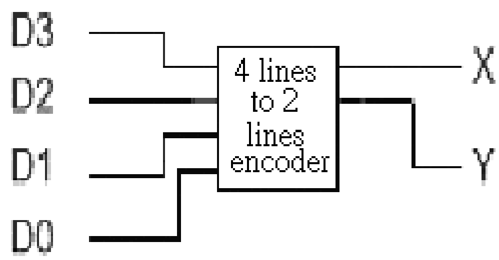
Figure 4-4, the switch encoder needs to operate with BCD code manually and send to digital system. The example is a calculator, when an operator presses a switch and sends a decimal number. In a basic calculator, every decimal number’s BCD code is sent to a 4 bits saver. In other words, when the first switch is pressed, the number’s BCD code is sent to a 4 bits FF temporary saver, when the second switch is pressed, the number’s BCD code is sent to another 4 bits FF temporary saver and so forth. Therefore, a calculator can handle eight numbers and save eight four-bit temporary saver’s BCD codes. And each four bits temporary saver drives one decoder/driver and number display. Therefore, the eight numbers can be displayed.



4 lines to 2 lines encoder

As figure 4-5 shows, 4 lines to 2 lines encoder can only respond one input at any time. The truth table shows binary output Boolean Algebra is

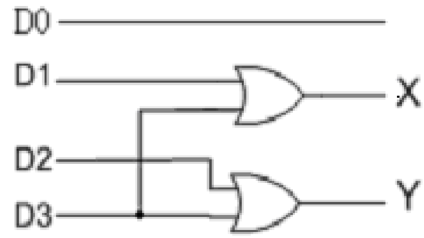
$$X=D_3+D_2$$
$$Y=D_3+D_1$$



(a) Square figure

Input				output	
D3	D2	D1	D0	X	Y
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

(b) Truth table



(C) Circuit

4 lines to 2 lines prior encoder

Figure 4-5 encoder can only accept one input at any time. If there is more than one input, then the encoder output is meaningless and useless. For example, when D1 and D2 are both 1 which makes encode output XY=1 wrong. To improve this disadvantage, we have to consider the input's priority, as figure 4-6's 4 to 2 priority encoder, D3 has the most priority and when there is more than one input as 1, it depends on the input priority, the truth table Boolean Algebra is:

$$X = \Sigma\,(4+5+6+7) + \Sigma\,(8+9+10+11+12+13+14+15)$$
$$= D_3 + D_2$$

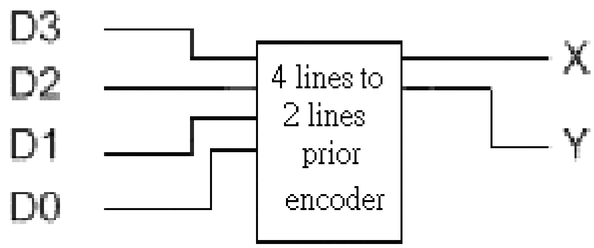
$$Y = \Sigma\,(2+3) + \Sigma\,(8+9+12+11+12+13+14+15)$$
$$= D_3 + \overline{D_2}\,D_1$$

D_3D_2 \ D_1D_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$X = D_3 + D_2$

D_3D_2 \ D_1D_0	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

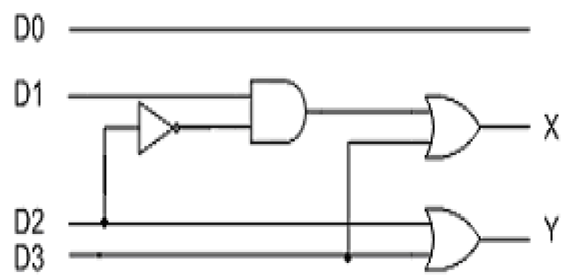
$Y = D_3 + \overline{D_2}D_1$



(a) Block Diagram

Input				Output	
D3	D2	D1	D0	X	Y
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

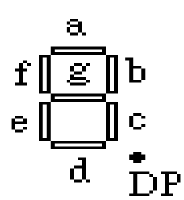
(b) Truth table



(c) Circuit

4-2-3 7 segment display 5 decoder's design

7-segment display plays a very important role in digital circuit appliance. Almost all the related display circuits have to use it. Therefore, there are all sorts of IC manufactured. Some IC only convert BCD input to 7 segment output which divides into two kinds: 1. specially designed for LED 7 segment display and 2. specially designed for LCD.



.The IC for LED 7 segment display has two kinds: one is applied on common negative pole's 7 segment display, such as 7448 (TTL) and 4511 (COMS). Another one is applied on common positive pole's 7 segment display, such as 7447. The difference between these two IC is that after they are decoded, each segment's output is 1 or 0 electronic potential. Because of LED's character, if we want to switch on LED, the electronic potential needs to be clockwise. Therefore, for common negative poles 7 segment display drive 1 electronic potential needs to be added; that is why 7448 and 4511 have decode output 1 as electronic potential. As for common positive pole's 7 segment display drive, we need to add 0 electronic potential, therefore 7447 decode output has 0 as electronic potential so that it can provide a clockwise direction to LED.

As 7 segment display has two forms, therefore there are two kinds of pushing circuits, but the decode theory is the same. In fact, the only difference is the reverser. such as 7448. Its circuit is the circuit output of 7447 plus one reverser. The design theory of 7447 is as follows:

1. Assume numbers from 0-15 displayed by 7 segment display as figure 4-7.

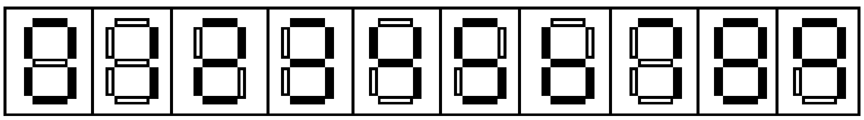


Figure 4-7 0-9's 7 segment

2. According to 7 segment display's figure, we list the truth table as table 4-1. Because 7447 has the character of active low, therefore when LED is on, the output is as 0.
3. The relationship of a, b, c, d, e, f, g's input and output, as figure 4-8's k-map

Table 4-1

FUNCTION	INPUT						OUTPUT								NOTE
	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	OFF	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	

8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	H	X	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	

Note: Assume output electronic potential is 0(also call active low) (as 7447), if we use common positive pole's LED, then the switch on is as its output 0 electronic potential. The truth table's on means 0 electronic potential, off means 1.

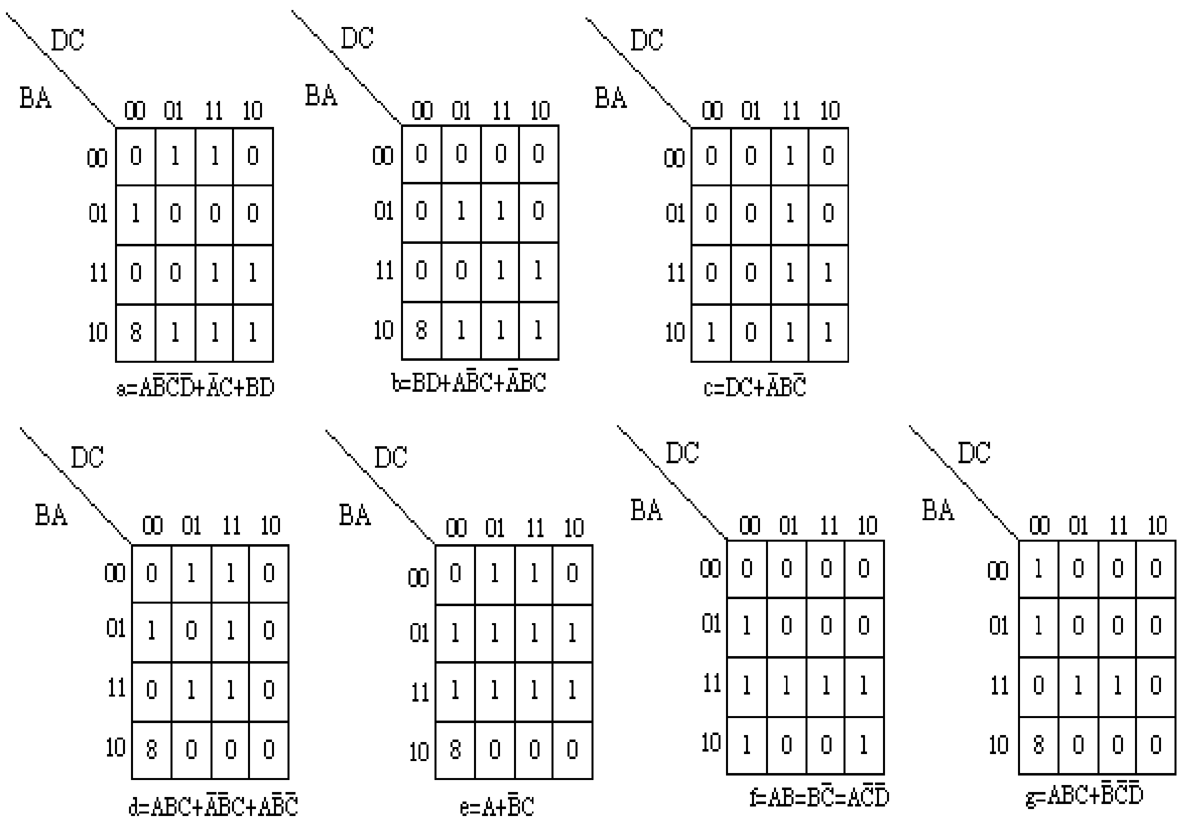


Figure 4-8 7 segment display decoder's simplified k-map

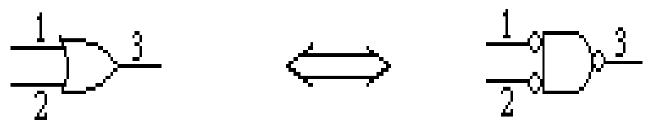
4. The result of k-map simplification:

$$a = A\bar{B}\bar{C}\bar{D} + \bar{A}C + BD$$
$$b = BD + A\bar{B}C + \bar{A}BC$$
$$c = CD + \bar{A}B\bar{C}$$

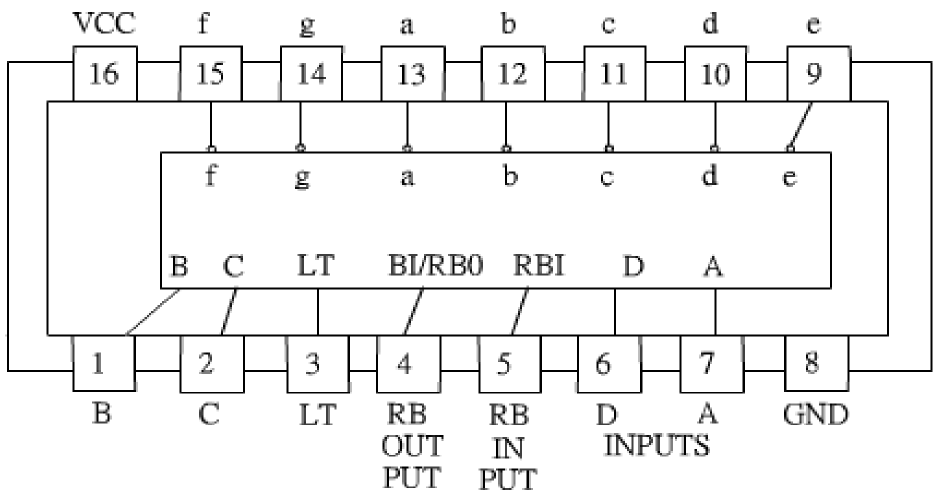
$$d = ABC + \overline{A}\,\overline{B}C + A\overline{B}\,\overline{C}$$
$$e = A + \overline{B}C$$
$$f = AB + B\overline{C} + A\overline{C}\,\overline{D}$$
$$g = ABC + \overline{B}\,\overline{C}\,\overline{D}$$

Logic circuit as figure 4-9 (b)

5. In figure 4-9 (b), OR gate is the result of negative input NAND gate, as follows:

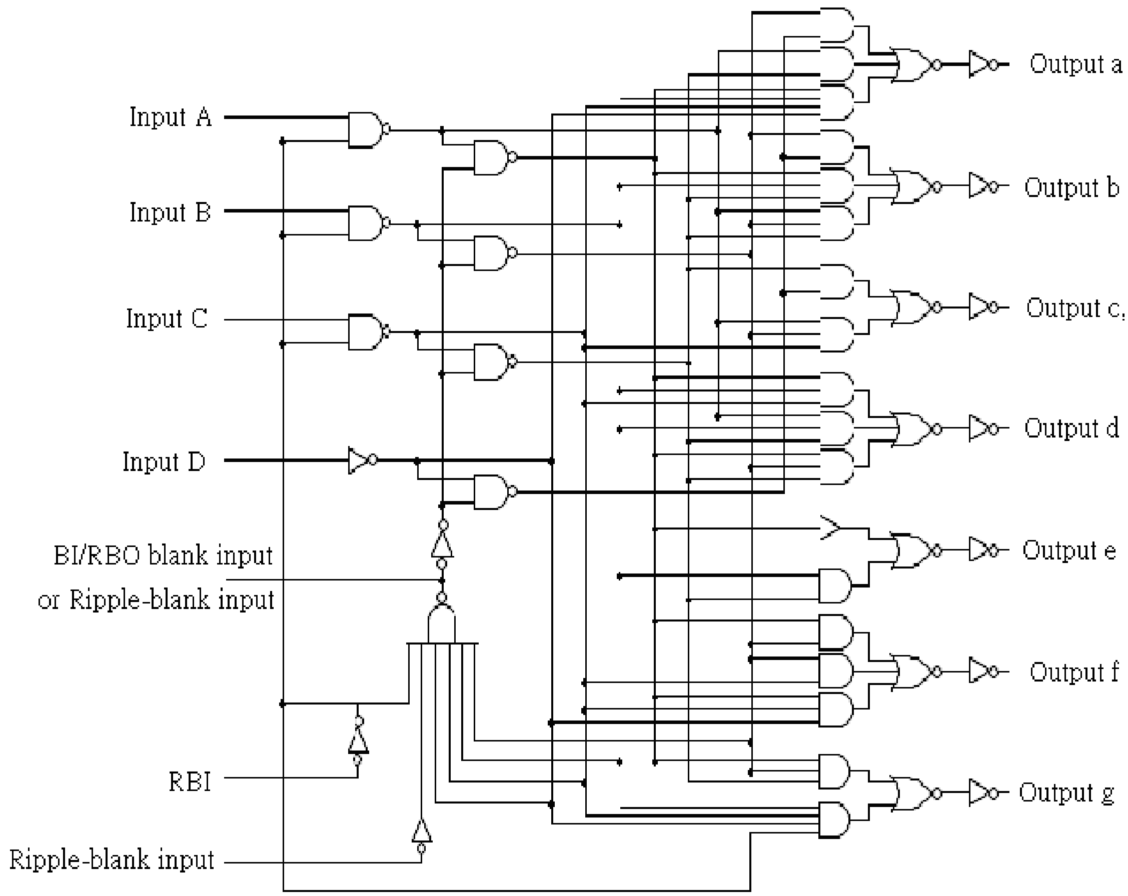


6. Figure 4-9 (b)'s circuit not only executes the results of "4", but also the following three control signal input functions:

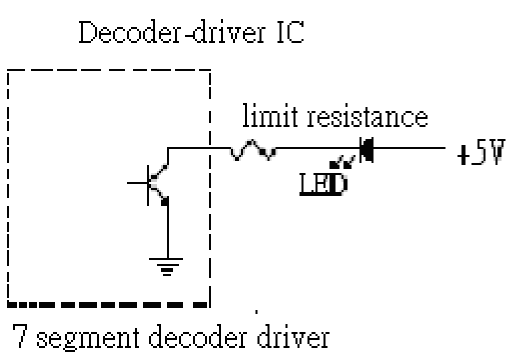


(a)

Figure 4-9 Typical 7 segment decoder – driver output and outer connection 1



(b) BCD to 7 segment decoder driver IC



(c)

Figure 4-9 Typical 7 segment decoder – driver output and outer connection

(a) Lamp test input, LT: The input function is to check 7-segment display's LED is functioning well or not. Therefore, when LT inputs 0 electronic potential, it makes 7 segment's output become 0 electronic potential, which is normal 7 segment LED display and it should show 8 numbers. Attention: It is effective only when BI/RBO stays 1 electronic potential, and LT is 0.

(b) Ripple-Blanking input, RBI: When the input is 0 electronic potential, the bit 0 is off.

(c) Blanking Input/ Ripple Blanking Output: It is often used when it is connected to +5v, if the end is 0 electronic potential, then all 7 segment output is 1 electronic potential and the display is off.

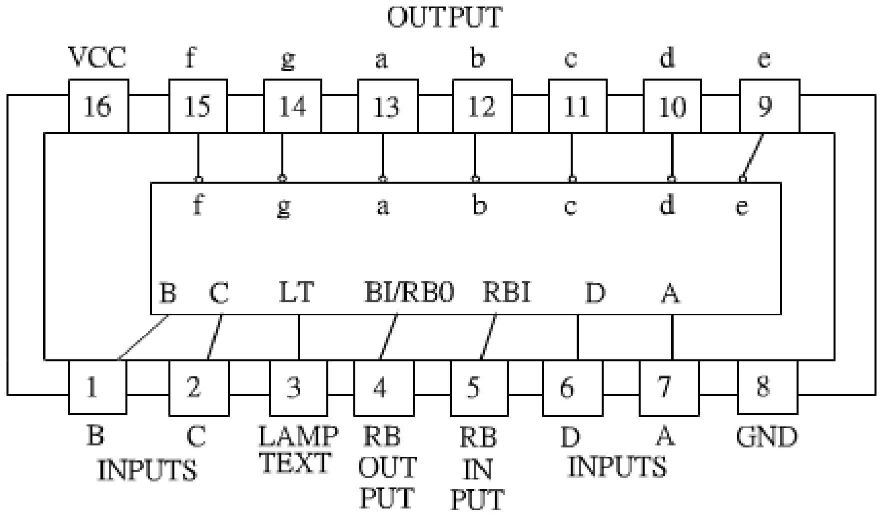
Push LCD 7 segment display decoder, such as CD4054, because its circuit's design is similar to 7447 and its output electronic potential is made for LED.

(1) 7447 is 8421BCD to 7-segment display, 7447 turns BCD to 7-segment output decoder; figure 4-10 is the connecting figure and truth table.

7447 pushes LED display's connecting is as figure 4-11. 7447's 7 output ends are a, b, c, d, e, f, and g. In figure 4-10, 7447's connection, we know that the third connecting end is lamp test. LT is active low, which means when the third connecting end is low; all the outputs are low as well. 7 segments display is on and we can check if each of LED's section is normal or not. 7447's fifth connecting end is ripple blanking input, when LT connects or does not connect to Hi, A, B, C, D have output low and RBI ends is Hi, then LED shows 0. If RBI (the fifth connecting end) is lows, then LED 7 sections are off. For example, if there is a 6 numbers display, we would like to see 2047, instead of 002047, if the first two 7 numbers display's light is not on, and then it shows 2047. 7447's fourth connecting end is blanking input remote blanking output. From its truth table, we know that if we add low to the fourth connecting end, then the 7 numbers display light is off, no matter what A, B, C, D are. Record "x" as Hi or Low is fine. If RBI and ABCD input are both low, then BI/ROB ends are low (7 number display light is off). If RBO output end connects to RBI input end, then when the next ABCD input is low, it display light is off. As figure 4-12, connecting the highest RBI, second highest BI/RBO's RBI, so forth. The lowest one is BI/RBO which is the opposite and RBI connects to BI/RBO, connecting to RBI.

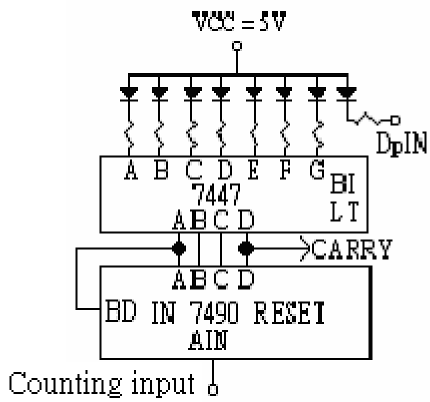
Function	INPUT						BI/	ON/OFF						
	LT	RBI	D	C	B	A	RBO	a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	H	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	ON	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
94	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

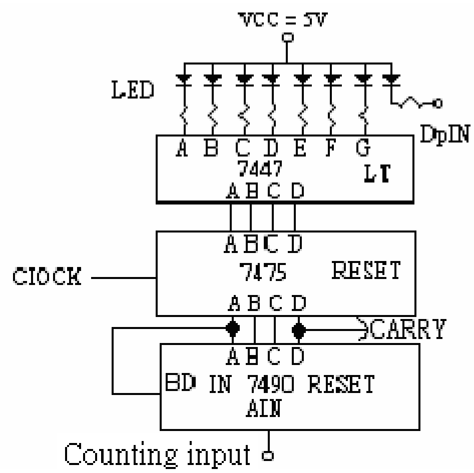
(b) Truth table



(a) Connection map

Figure 4-10





(a) (b)

Figure 4-11 7447 Push 7 segment LED display

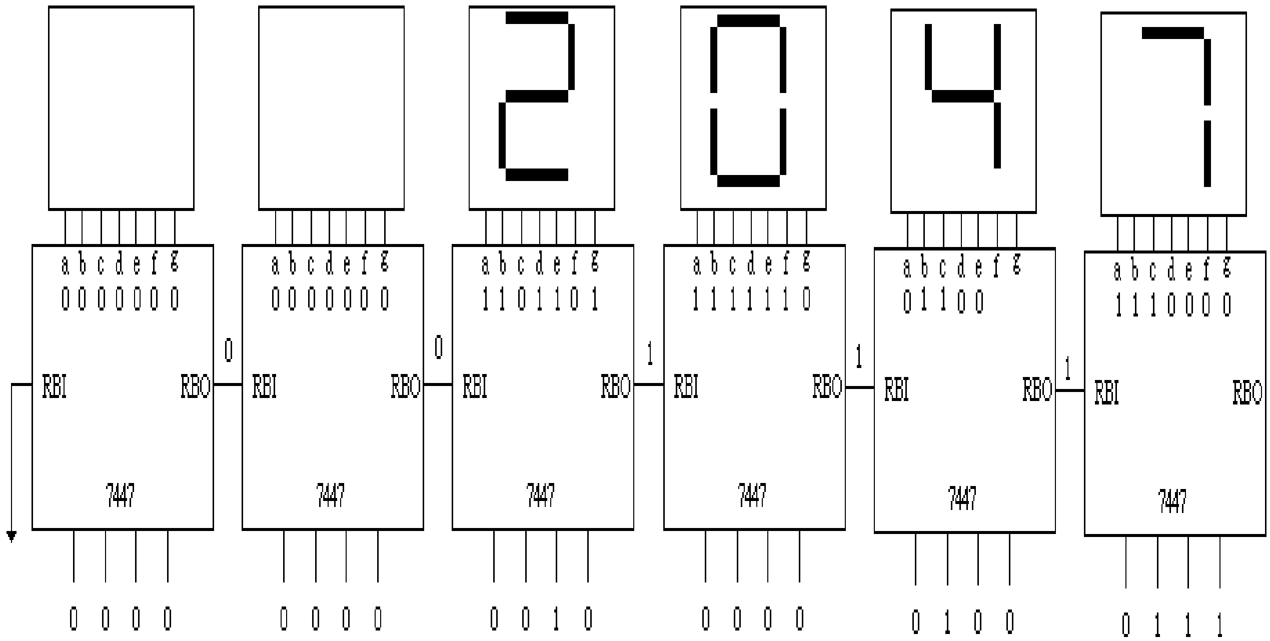


Figure 4-12 Blank 0 space display – number 2047

(2) 7448 is BCD to 7-segment decoder/driver. Figure 4-3 is its figure and its function is exactly the same as 7447, just that the output is high output push common negative 7-segment display which is opposite to 7447's. Its method and pushing display character is the same as 7447's. Learners please pay attention to 7 segment output, a, b, c, d, e, f, g ends to see the difference between with or without the small circle.

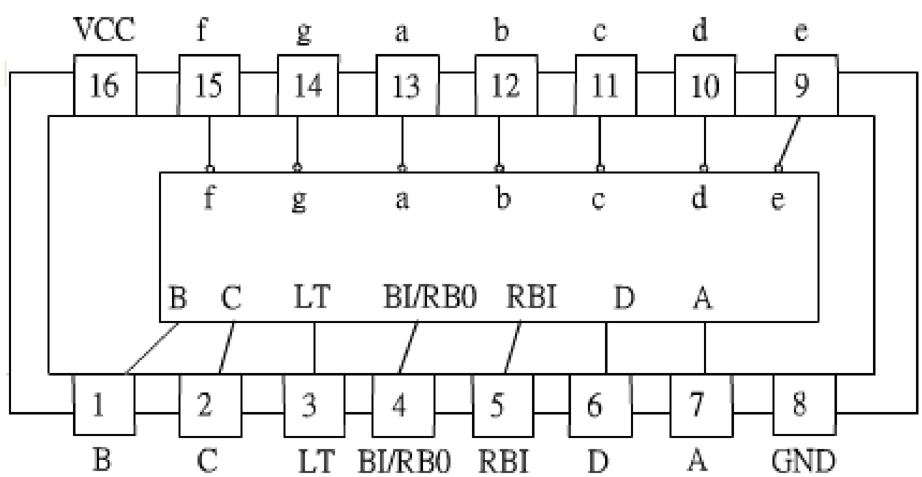


Figure 4-13

4-3 Practice items

4-3-1
Experiment steps

1. 2 to 4 decoder circuit as figure 4-14.

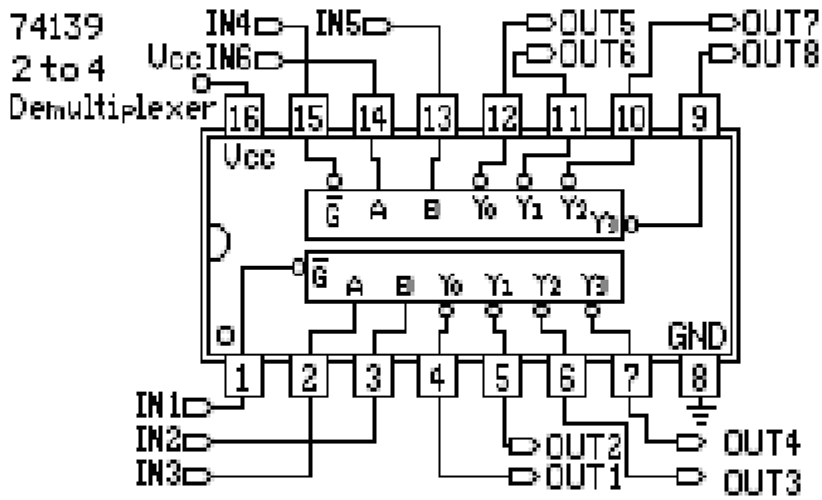


Figure 4-14

2. Input: Connect CON7 S1 to CON1 IN1.
   Connect CON7 S2 to CON1 IN2
   Connect CON7 S3 to CON1 IN3
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q9
   Connect CON4 OUT2 to LED DISPLAY CON15 Q10
   Connect CON4 OUT 3 to LED DISPLAY CON15 Q11
   Connect CON4 OUT4 to LED DISPLAY CON15 Q12
3. Switch S1, S2 and S3 after finished connecting, as table 4-2. 0 means low logic LED off, 1 means high logic, LED on.
4. Record LED changes in Table 4-2.

G(S1)	B(S2)	A(S3)	Y_0 Y_1 Y_2 Y_3
1	X	X	
0	0	0	
0	0	1	
0	1	0	
0	1	1	

Table 4-2

4-3-2

1. Common positive 7 segment display circuit, as figure 4-15

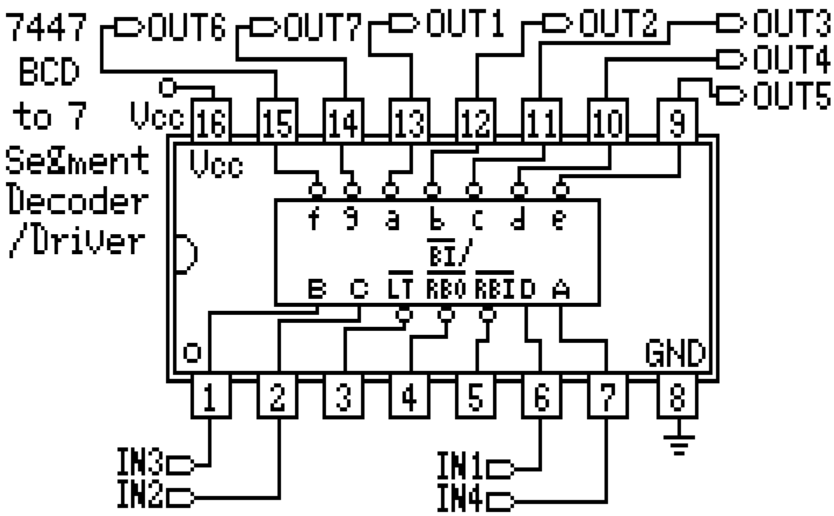


Figure 4-15

2. Input: Connect CON7 S1 to CON1 IN1.
   Connect CON7 S2 to CON1 IN2
   Connect CON7 S3 to CON1 IN3
   Connect CON7 S4 to CON1 IN4
   Output: Connect CON4 OUT1 to 7-SEGMENT CON10 LED 1a
   Connect CON4 OUT2 to 7-SEGMENT CON10 LED 1b
   Connect CON4 OUT3 to 7-SEGMENT CON10 LED 1c
   Connect CON4 OUT4 to 7-SEGMENT CON10 LED 1d
   Connect CON4 OUT5 to 7-SEGMENT CON10 LED1 e
   Connect CON4 OUT6 to 7-SEGMENT CON10 LED1 f
   Connect CON4 OUT7 to 7-SEGMENT CON10 LED1 g
3. Switch S1, S2 S3 and S4 after finished connecting, as table 4-3, 0 means low logic LED off, 1 means high logic, LED on.
4. Record LED changes in Table 4-3.

Input							Display result
$\overline{LT}$	$\overline{BI}/\overline{RBO}$	$\overline{RBI}$	D (S1)	C (S2)	B (S3)	A (S4)	
x	0	x	x	x	x	x	
0	1	x	x	x	x	x	
1	1	0	0	0	0	0	
1	1	1	0	0	0	0	
1	1	1	0	0	0	1	
1	1	1	0	0	1	0	
1	1	1	0	0	1	1	
1	1	1	0	1	0	0	
1	1	1	0	1	0	1	
1	1	1	0	1	1	0	
1	1	1	0	1	1	1	
1	1	1	1	0	0	0	
1	1	1	1	0	0	1	
1	1	1	1	0	1	0	
1	1	1	1	0	1	1	
1	1	1	1	1	0	0	
1	1	1	1	1	0	1	
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	

Table 4-3

4-3-3

Experiment steps

1. 4 to2 decoder circuit as figure 4-16.

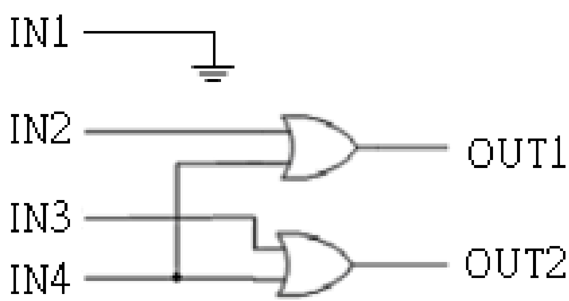


Figure 4-16

2. Input: Connect CON7 S1 to CON1 IN1.
   Connect CON7 S2 to CON1 IN2
   Connect CON7 S3 to CON1 IN3
   Connect CON7 S4 to CON1 IN4

   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1
   Connect CON4 OUT2 to LED DISPLAY CON15 Q2

3. Switch S1, S2 S3 and S4 after finished connecting, as table 4-4. 0 means low logic LED off, 1 means high logic, LED on.
4. Record LED changes in Table 4-4.

Input				Output	
IN4 S4	IN3 S3	IN2 S2	IN1 S1	OUT2 Q2	OUT1 Q1
0	0	0	1		
0	0	1	0		
0	1	0	0		
1	0	0	0		

Table 4-4

4-3-4

Experiment steps

1. 4 to 2 priority encoder circuit, as figure 4-17.

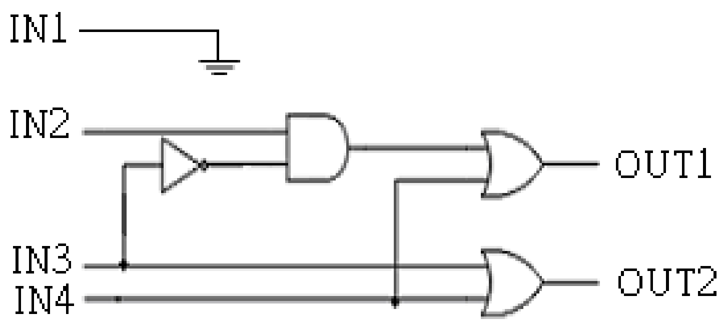


Figure 4-17

2. Input: Connect CON7 S1 to CON1 IN1.
   Connect CON7 S2 to CON1 IN2
   Connect CON7 S3 to CON1 IN3
   Connect CON7 S4 to CON1 IN4
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1
   Connect CON4 OUT2 to LED DISPLAY CON15 Q2
3. Switch S1 to S4 after finished connecting, as table 4-5. 0 means low logic LED off, 1 means high logic, LED on.
4. Record LED changes in Table 4-5.

Input				Output	
IN4 S4	IN3 S3	IN2 S2	IN1 S1	OUT2 Q2	OUT1 Q1
0	0	0	1		
0	0	1	0		
0	1	0	0		
1	0	0	0		

Table 4-5

4-3-5

Experiment steps

1. 3 to 8 decoder circuit, as figure 4-18

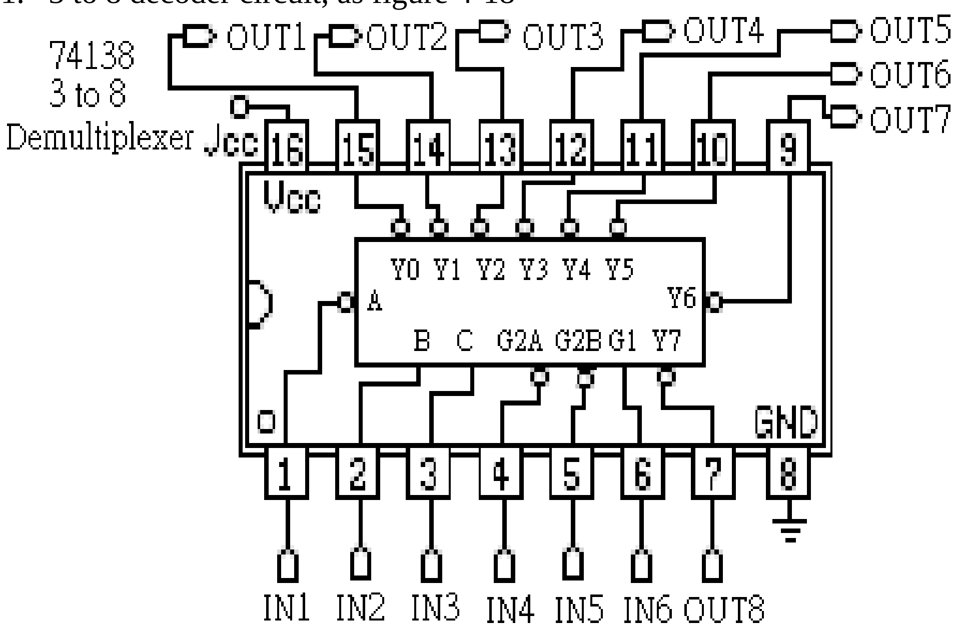


Figure 4-18

2. Input: Connect CON7 S1 to CON1 IN1.
   Connect CON7 S2 to CON1 IN2
   Connect CON7 S3 to CON1 IN3
   Connect CON7 S4 to CON1 IN4
   Connect CON7 S5 to CON1 IN5
   Connect CON7 S6 to CON1 IN6
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q9
   Connect CON4 OUT2 to LED DISPLAY CON15 Q10
   Connect CON4 OUT 3 to LED DISPLAY CON15 Q11

Connect CON4 OUT4 to LED DISPLAY CON15 Q12
Connect CON4 OUT5 to LED DISPLAY CON15 Q13
Connect CON4 OUT6 to LED DISPLAY CON15 Q14
Connect CON4 OUT7 to LED DISPLAY CON15 Q15
Connect CON4 OUT8 to LED DISPLAY CON15 Q16

3. Switch S1 to S8 after finished connecting, as table 4-6. 0 means low logic LED off, 1 means high logic, LED on.
4. Record LED changes in Table 4-6.

G1 G2” S6(S5+S4)	C B A S3 S2 S1	Y0 Q9	Y1 Q10	Y2 Q11	Y3 Q12	Y4 Q13	Y5 Q14	Y6 Q15	Y7 Q16
X 1	X X X	0	0	0	0	0	0	0	0
0 X	X X X	0	0	0	0	0	0	0	0
1 0	0 0 0	1	0	0	0	0	0	0	0
1 0	0 0 1	0	1	0	0	0	0	0	0
1 0	0 1 0	0	0	1	0	0	0	0	0
1 0	0 1 1	0	0	0	1	0	0	0	0
1 0	1 0 0	0	0	0	0	1	0	0	0
1 0	1 0 1	0	0	0	0	0	1	0	0
1 0	1 1 0	0	0	0	0	0	0	1	0
1 0	1 1 1	0	0	0	0	0	0	0	1

Table 4-6

Ps. ： G2”＝G2A＋G2B
X ＝ irrelevant

4-4 Questions & Discussion

1. What is the difference between an encoder and a decoder?
2. How many inputs are there from 1-16 demultiplexer?