

## Chapter 3 Arithmetic Circuit Practice

### 3-1 The purpose of practice

1. To understand binary system addition and subtraction
2. To understand BCD addition and subtraction
3. To understand the usage of arithmetic ALU

### 3-2 Practice theory

One of the functions of logic circuit is the extreme speed in calculating arithmetic logic operations, which includes addition, subtraction, multiplication and division and the basic logic operation of AND, OR, NAND, and NOR. The arithmetic operations are based on addition and subtraction. We can also say that all the operations are based on addition operation, multiplication is a series of addition, subtraction is operated with 1 and 2's supplement and division is a series of subtraction.

As the digits to show numbers are different, does this make the operations different as well? The operation rule is called BCD operation when the numbers are shown with the binary system.

The following is a discussion on many kinds of circuit operations, including how to use ALU IC as well.

#### 3-2-1 The design of adder

A calculator can deal with very complicated mathematical operations and the most basic ones are arithmetic operations, which also have the most basic calculation, addition and subtraction. In fact, an adder is the basis of all the operations. For example, multiplication is a series of addition, subtraction is a supplement plus 2, and division is a series of subtraction.

As the digits of operation numbers are different this makes the operation different as well. Therefore, the operation rule with two binary system numbers is called binary operation and the ones with BCD codes are called BCD operation.

Examples of binary addition are as follows:

$$0+0=0$$

$$0+1=1$$

$$1+0=1$$

$$1+1=10$$

The first three operations have only one digit total, but when the first and the second digits are both 1, the total becomes two digits in which the higher bit is called carrying. If there is a higher bit than the original one, then the carrying one is added as well.

Therefore, the adder for only two bits is called Half adder, but if there are more than two bits, then it is called Full adder.

When the added bits are multiple, there will be many designs. Figure 3-1 is half adder, there are two outputs, two inputs, the input variables, x and y, are added number and adding number, the output variables have a total of S and carrying C. See figure 3-1(b).

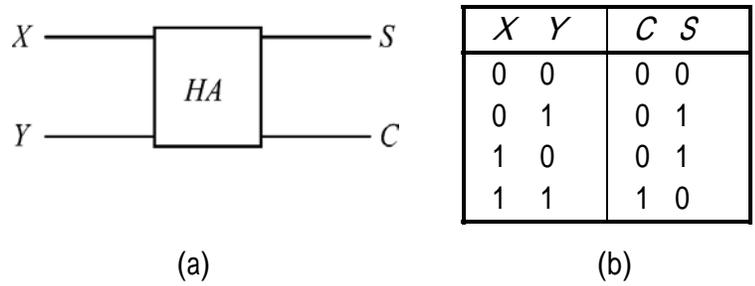
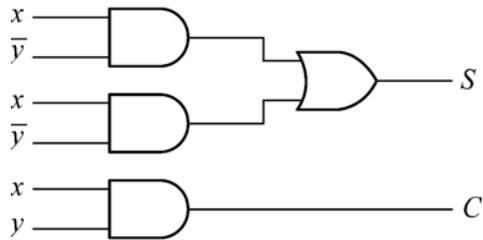


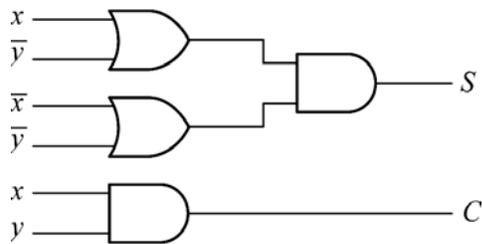
Figure 3-1

The result of following half adders

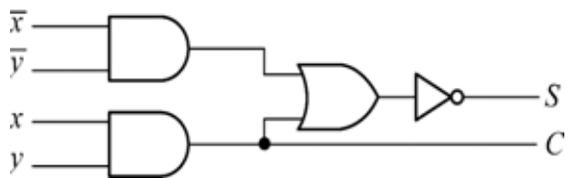
(1)  $S = \bar{x}y + x\bar{y}$   
 $C = xy$



(2)  $S = (x+y)(\bar{x} + \bar{y})$   
 $C = xy$

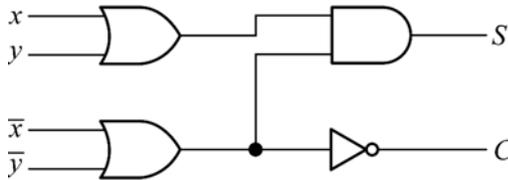


(3)  $\bar{S} = xy + \bar{x}\bar{y}$   
 $S = \overline{(C + xy)}$   
 $C = xy$



$$(4) S = (x+y)(\bar{x} + \bar{y})$$

$$C = \overline{(x+y)}$$



$$(5) S = x \oplus y$$

$$C = xy$$

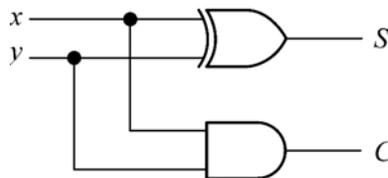
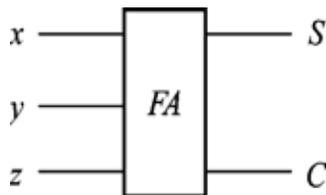


Figure 3-2 Half adder circuit

- Full adder

Full adder is a combinational circuit which can complete the total of three input bits arithmetic. As figure 3-3(a), there are three inputs and two outputs, which x and y show two effective input bit variables. The third input, z, shows the lower effective carrying. It is necessary to have two outputs, because the total of three binary arithmetic can be from 9 to 3, and 2 and 3 in binary need two digits which show symbol S as total and C as carrying. The full adder's truth figure is as figure 3-3(b).



(a)

Z	X	Y	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b)

Figure 3-3

Full adder form as follows:

$$(1) S = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$$

$$C = xy + xz + yz$$

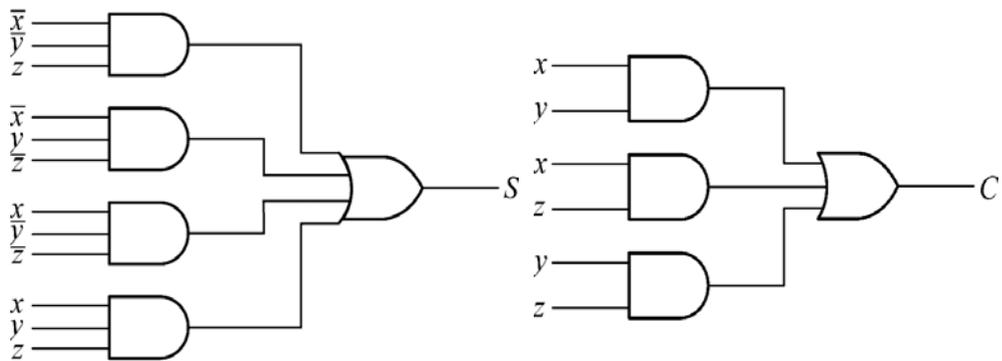


Figure 3-4

$$(2) S = z \oplus (x \oplus y)$$

$$= \bar{z}(x\bar{y} + \bar{x}y) + z(\overline{x\bar{y} + \bar{x}y})$$

$$= \bar{z}(x\bar{y} + \bar{x}y) + z(xy + \bar{x}\bar{y})$$

$$= x\bar{y}\bar{z} + \bar{x}y\bar{z} + xyZ + \bar{x}\bar{y}Z$$

$$C = z(x\bar{y} + \bar{x}y) + xy = x\bar{y}z + \bar{x}yZ + xy$$

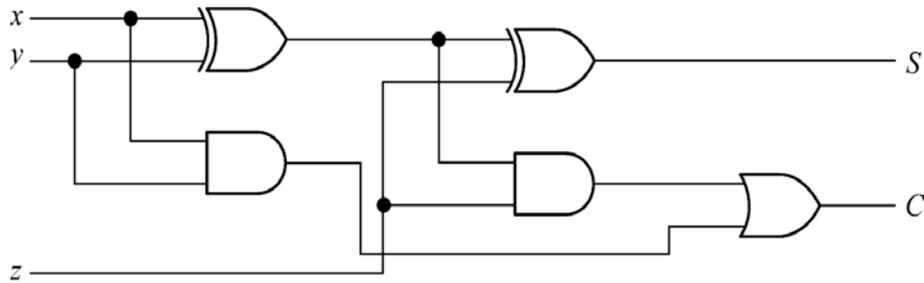


Figure 3-5

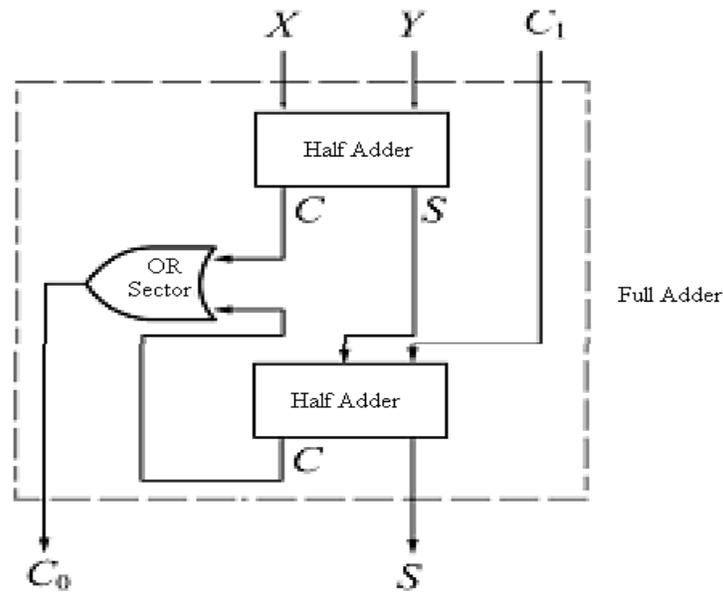


Figure 3-6

### 3-2-2 Subtractor

Adding subtractor's complement adds subtracted number can be the two binary digits' subtraction. By using this method, subtraction becomes addition and for its machine manufacturing, we need full adder to complete. Sometimes to omit the procedure, we can also use logic circuit directly manufacture subtractor.

Subtractor is like adder. There are half subtractor and full subtractor.

#### 1. Half subtractor

Half subtractor is as figure 3-7(a) and 3-7(b) is truth figure and its output equation.

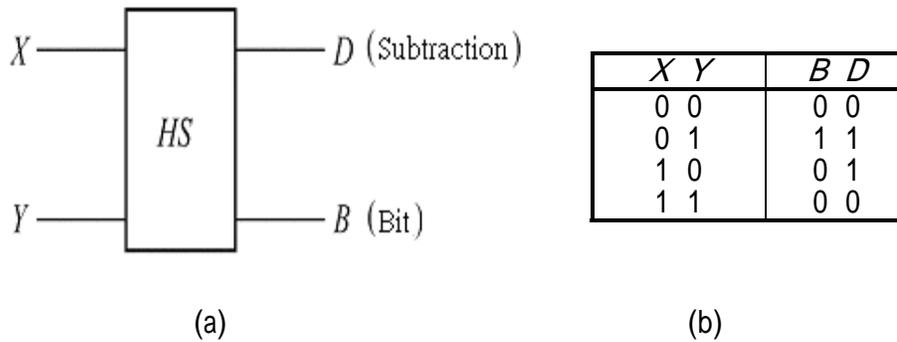


Figure 3-7

As for B, we can tell that  $x \geq y$ , the value is 0, if  $x=0, y=1$ , and its value is 1, at the same time, the difference bit D is 1 which means it has the same meaning as denary's xxxx.

## 2. Full subtractor

Full subtractor is more practical than half subtractor.

Full subtractor has the function of completing one low bit's borrowing bit numbers when the original bit is doing calculation. And after that, the subtraction is proceeded with. Therefore, there are three input ends,  $B_{IN}$ ,  $x$ , and  $y$ . Figure 3-8 explains the subtraction of output D and borrowing bit B.

When  $B_{IN}$  is 0 which is the same as the four situations of half subtractor and  $B_{IN}$  is 1,  $x=0$ , and  $y=0$ , we have to borrow 1 from the next low bit. So when the B output is 1,  $B=1$ , X bit is 2, therefore,  $2-0-1=1$ , the difference bit D is 1. Vice verse to the other three situations.

## 3-2-3

### BCD adder

The adding numbers mentioned, added numbers, subtracting numbers, subtracted numbers all apply the binary system or the supplement form ( 2 or 1 supplement) to express, the operation result is shown with this number system. But most of the number displays use the decimal system which is easier to see. Therefore, such as things as calculators, digital electronic press gauges, electronic thermometers all apply the decimal system, that is why there is one more binary conversion procedure. But, sometimes we can directly use the decimal system to express the operation, which has to first convert all the numbers to BCD (binary-coded decimal), and use four binary bits to replace the one bit in decimal system. For example,  $64_{10}$  (the small, lower right characters are decimal system) shown by the binary system is:

We can tell that these two presentations are totally different, which results in different operations. In general, BCD operation is more complicated than binary operation, but it is very easy to convert to the decimal system.

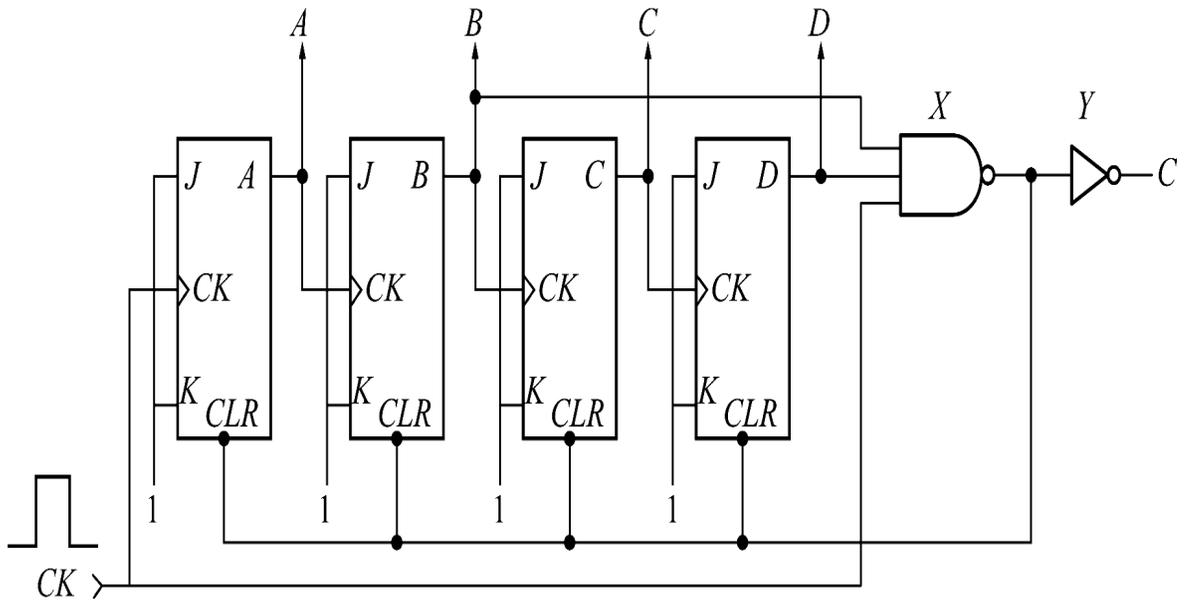
To show numbers with four binary systems, usually we can do it from 0-15, but BCD can only operate from 0-9 (0000<sub>2</sub>-1001<sub>2</sub>), 1- combinational. Therefore, for our convenience, one unit becomes decimal system's one bit converted to four binary systems, and from this unit we know that when it counts to 10 or over 10, it returns to 0. This combinational is much like combining with calculators and dividing with 10's circuit. Therefore, we can combine BCD's basic units with positive and negative operator. Figure 3-9 is one unit BCD combined with non-synchronization and its logic symbol is as figure (b). When B(2<sub>1</sub>), D(2<sub>3</sub>) is 1, and the order wave come into number ten, NAND gate set up is 0 which makes each positive and negative operator's CL end affected and turn A, B, C, D, to 0. Also NAND gate's output gets 1 output through the positive and negative operator, and then turns to carrying end (C).

If we want to show three numbers' decimal system with BCD basic units, we can divide it by 10 counters connecting to three of them. Figure 3-10 is single BCD logic symbol with three connections. So N unit BCD counter can make N decimal system so that when it comes to 9, there is one carrying, shown as figure 3-11.

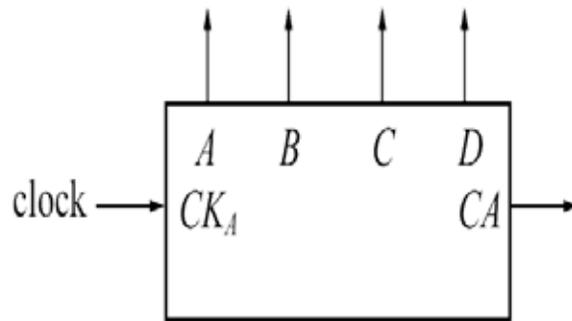
<i>X</i>	<i>Y</i>	<i>B<sub>IN</sub></i>	<i>B</i>	<i>D</i>
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure 3-8

### 3-2-3 BCD adder



(a) Asynchronous BCD counter



(b) Logic figure

Figure 3-9

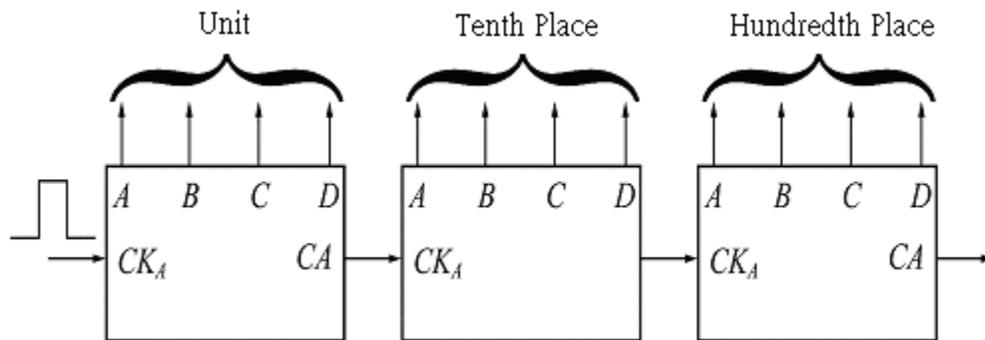


Figure 3-10 Asynchronous BCD counter

Figure 3-11

Decimal system	BCD							
	The tenth place				a unit			
	D	C	B	A	D	C	B	A
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	<u>1</u>	<u>0</u>	<u>0</u>	<u>1</u>
10	0	0	0	1	0	0	0	0
11	0	0	0	1	0	0	0	1
12	0	0	0	1	0	0	1	0
13	0	0	0	1	0	0	1	1
14	0	0	0	1	0	1	0	0
15	0	0	0	1	0	1	0	1
16	0	0	0	1	0	1	1	0
17	0	0	0	1	0	1	1	1
18	0	0	0	1	1	0	0	0
19	0	0	0	1	<u>1</u>	<u>0</u>	<u>0</u>	<u>1</u>
20	0	0	1	0	0	0	0	0
21	0	0	1	0	0	0	0	1

When a unit reaches 9, it moves to the tenth place

When a unit reaches 9, it moves to the tenth place

The tenth place	Before amendment		After amendment	
	Carrying $\overline{C_4}$	$\overline{S_4 S_3 S_2 S_1}$	Carrying $C_n$	Total $S_4 S_3 S_2 S_1$
0		0 0 0 0		0 0 0 0
1		0 0 0 1		0 0 0 1
2		0 0 1 0		0 0 1 0
3		0 0 1 1		0 0 1 1
4		0 1 0 0		0 1 0 0
5		0 1 0 1		0 1 0 1
6		0 1 1 0		0 1 1 0
7		0 1 1 1		0 1 1 1
8		1 0 0 0		1 0 0 0
9		1 0 0 1		1 0 1 0
10		1 0 1 0	1	1 0 1 1
11		1 0 1 1	1	1 1 0 0
12		1 1 0 0	1	1 1 0 1
13		1 1 0 1	1	1 1 1 0
14		1 1 1 0	1	1 1 1 1
15		1 1 1 1	1	0 1 1 1
16	1	0 0 0 0	1	0 1 0 0
17	1	0 0 0 1	1	0 1 0 1
18	1	0 0 1 0	1	1 0 1 0
19	1	0 0 1 1	1	1 0 1 1

No supplement when total is less than 9

Supplement needed when total is over 9 (plus 6)

Figure 3-12 result of 2 BCD digits addition

		$\overline{S_2} \overline{S_1}$		
			00	01
$\overline{S_4} \overline{S_3}$			11	10
	00			
	01			
	11	(1	(1	(1
	10		(1	(1

Figure3-13  $C_n = \overline{C_4} + \overline{S_4} \overline{S_3} + \overline{S_4} \overline{S_2}$

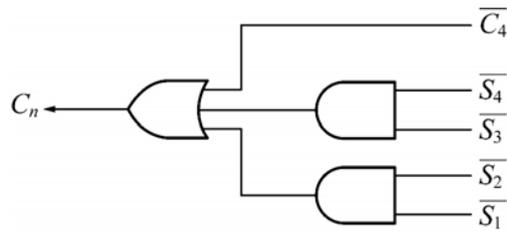
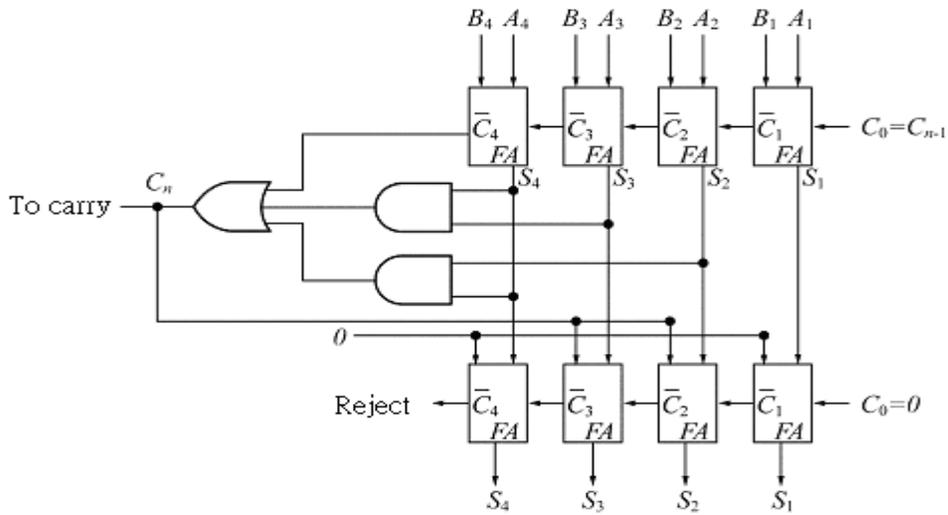
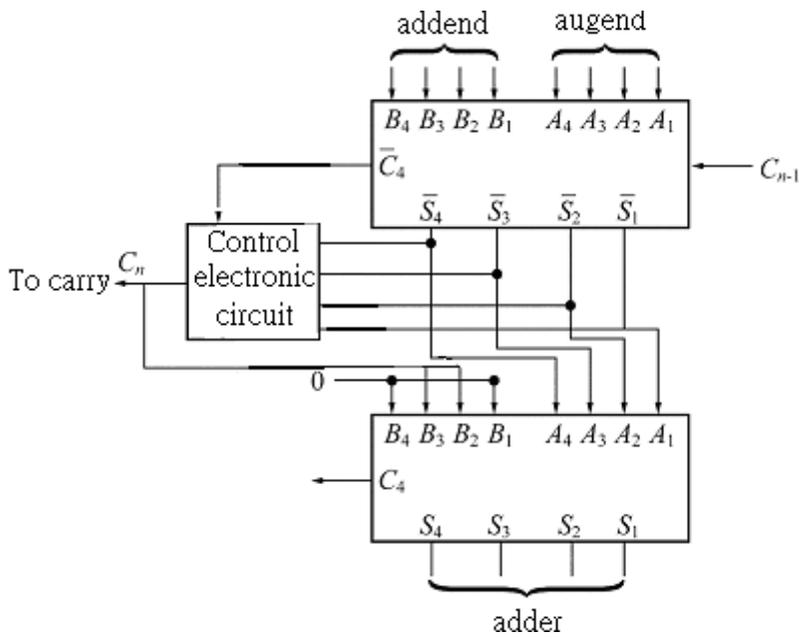


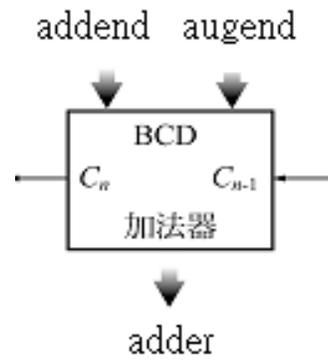
Figure3-14 BCD carrying control circuit



(a)



(b)



(c)

Figure3-15 BCD adder

### 3-3 Practice items

3-3-1

Experiment steps

1. Half adder circuit as figure 3-16.

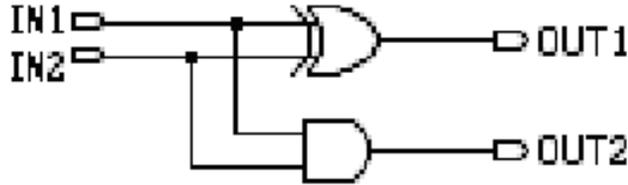


Figure 3-16

2. Input: Connect CON7 S1 to CON1 IN1  
Connect CON7 S2 to CON1 IN2  
Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1  
Connect CON4 OUT2 to LED DISPLAY CON15 Q2
3. Switch S1, S2, as table 3-1. 0 means low logic, LED off, 1 means high logic, LED on.
4. Record LED changes in table 3-1

A(S1)	B(S2)	C(Q2)	S(Q1)
0	0		
0	1		
1	0		
1	1		

Table 3-1

3-3-2

Experiment steps

1. Full adder circuit, as figure 3-17.

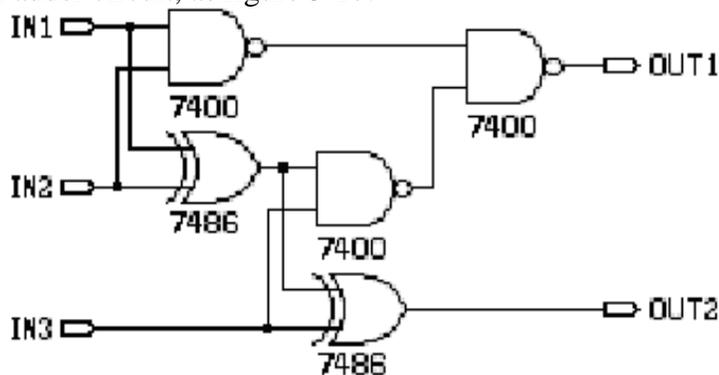


Figure 3-17



4. Record LED changes in table 3-3.

X(S1)	Y(S2)	B(Q2)	D(Q1)
0	0		
0	1		
1	0		
1	1		

Table 3-3

3-3-4

Experiment steps

1. Full subtractor circuit, as figure 3-19.

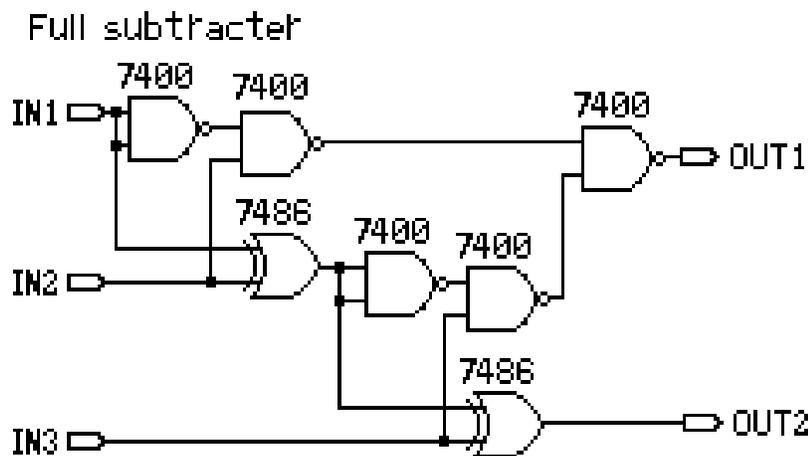


Figure 3-19

2. Input:

- Connect CON7 S1 to CON1 IN1
- Connect CON7 S2 to CON1 IN2
- Connect CON7 S3 to CON1 IN3
- Connect CON7 A1 to CON3 B1
- Connect CON7 A2 to CON3 B2
- Connect CON7 A3 to CON3 B3
- Connect CON7 A4 to CON3 B4
- Connect CON7 A5 to CON3 B5
- Connect CON7 A6 to CON3 B6

Output:

- Connect CON4 OUT1 to LED DISPLAY CON15 Q1
- Connect CON4 OUT 2 to LED DISPLAY CON15 Q2

3. Switch S1, S2, and S3 as table 3-4. 0 means low logic, LED off, 1 means high logic, LED on.

4. Record LED changes in table 3-4.

X(S1)	Y(S2)	Z(S3)	B(Q1)	D(Q2)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 3-4

3-3-5

Experiment steps

1. Four bits adder/Subtractor circuit, as figure 3-20.

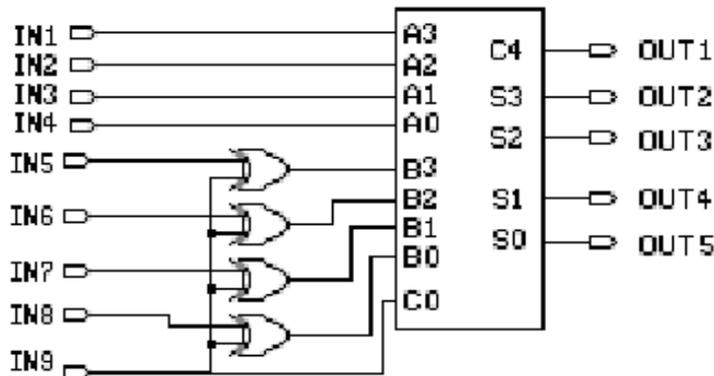


Figure 3-20

2. Input:  
 Connect CON7 S1 to CON1 IN1  
 Connect CON7 S2 to CON1 IN2  
 Connect CON7 S3 to CON1 IN3  
 Connect CON7 S4 to CON1 IN4  
 Connect CON7 S5 to CON1 IN5  
 Connect CON7 S6 to CON1 IN6  
 Connect CON7 S7 to CON1 IN7  
 Connect CON7 S8 to CON1 IN8  
 Connect CON6 S9 to CON1 IN9

Output:  
 Connect CON4 OUT1 to LED DISPLAY CON15 Q1  
 Connect CON4 OUT 2 to LED DISPLAY CON15 Q2  
 Connect CON4 OUT3 to LED DISPLAY CON15 Q3  
 Connect CON4 OUT4 to LED DISPLAY CON15 Q4  
 Connect CON4 OUT5 to LED DISPLAY CON15 Q5

3. Switch S1 to S9 as table 3-5. 0 means low logic, LED off, 1 means high logic, LED on.

4. Record LED changes in table 3-5.

E (S9)	A <sub>3</sub> (S1)	A <sub>2</sub> (S2)	A <sub>1</sub> (S3)	A <sub>0</sub> (S4)	B <sub>3</sub> (S5)	B <sub>2</sub> (S6)	B <sub>1</sub> (S7)	B <sub>0</sub> (S8)	C <sub>4</sub> (Q1)	S <sub>3</sub> (Q2)	S <sub>2</sub> (Q3)	S <sub>1</sub> (Q4)	S <sub>0</sub> (Q5)
0	0	0	0	1	1	1	1	1					
0	0	0	1	0	1	1	0	1					
0	0	0	1	1	1	0	1	1					
0	0	1	0	0	1	0	0	1					
0	0	1	0	1	0	1	1	1					
0	0	1	1	0	0	1	0	1					
0	0	1	1	1	0	0	1	1					
0	1	0	0	0	0	0	0	1					
0	1	0	0	1	1	1	0	0					
0	1	0	1	0	1	0	1	0					
0	1	0	1	1	1	0	0	0					
0	1	1	0	0	0	1	1	0					
0	1	1	0	1	0	1	0	0					
0	1	1	1	0	0	0	1	0					
0	1	1	1	1	0	0	0	0					
0	0	0	0	0	1	1	1	0					
1	0	0	0	1	1	1	1	1					
1	0	0	1	0	1	1	0	1					
1	0	0	1	1	1	0	1	1					
1	0	1	0	0	1	0	0	1					
1	0	1	0	1	0	1	1	1					
1	0	1	1	0	0	1	0	1					
1	0	1	1	1	0	0	1	1					
1	1	0	0	0	0	0	0	1					
1	1	0	0	1	1	1	0	0					
1	1	0	1	0	1	0	1	0					
1	1	0	1	1	1	0	0	0					
1	1	1	0	0	0	1	1	0					
1	1	1	0	1	0	1	0	0					
1	1	1	1	0	0	0	1	0					
1	1	1	1	1	0	0	0	0					
1	0	0	0	0	1	1	1	0					

Table 3-5

5. When E=0, circuit operates addition, when E=1, circuit operates subtraction. If C<sub>4</sub>=1 which means the result of subtraction is positive. If C<sub>4</sub>=0, which means negative. In table 3-5, is the result of the addition of input A and B the same as the experiment?

3-3-6

Experiment steps

1. BCD addition/subtraction circuit, as figure 3-21

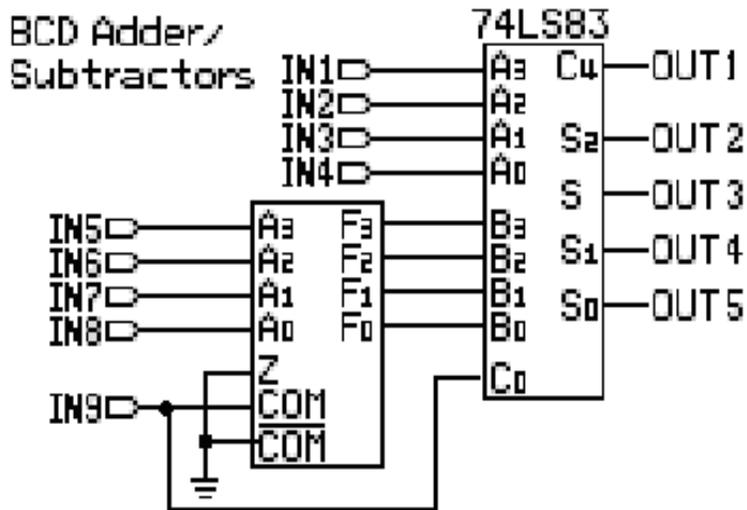


Figure 3-21

2. Input:
  - Connect CON7 S1 to CON1 IN1
  - Connect CON7 S2 to CON1 IN2
  - Connect CON7 S3 to CON1 IN3
  - Connect CON7 S4 to CON1 IN4
  - Connect CON7 S5 to CON1 IN5
  - Connect CON7 S6 to CON1 IN6
  - Connect CON7 S7 to CON1 IN7
  - Connect CON7 S8 to CON1 IN8
  - Connect CON6 S9 to CON1 IN9
  - Fix CON6 S10 as low  
(Meaning Connect CON6 B bar to CON1 IN10)Output:
  - Connect CON4 OUT1 to LED DISPLAY CON15 Q1
  - Connect CON4 OUT 2 to LED DISPLAY CON15 Q2
  - Connect CON4 OUT3 to LED DISPLAY CON15 Q3
  - Connect CON4 OUT4 to LED DISPLAY CON15 Q4
  - Connect CON4 OUT5 to LED DISPLAY CON15 Q5

3. Switch S1 to S9 as table 3-6. 0 means low logic, LED off, 1 means high logic, LED on.

4. Record LED changes in table 3-6.

E (S9)	A <sub>3</sub> (S1)	A <sub>2</sub> (S2)	A <sub>1</sub> (S3)	A <sub>0</sub> (S4)	B <sub>3</sub> (S5)	B <sub>2</sub> (S6)	B <sub>1</sub> (S7)	B <sub>0</sub> (S8)	C <sub>4</sub> (Q1)	S <sub>3</sub> (Q2)	S <sub>2</sub> (Q3)	S <sub>1</sub> (Q4)	S <sub>0</sub> (Q5)
0	0	0	0	1	0	0	1	0					
0	0	0	1	0	0	1	0	0					
0	0	0	1	1	0	1	1	0					
0	0	1	0	0	1	0	0	0					
0	0	1	0	1	1	0	1	0					
0	0	1	1	0	1	1	0	0					
0	0	1	1	1	1	1	1	0					
0	1	0	0	0	0	0	0	0					
0	1	0	0	1	0	0	0	1					
0	1	0	1	0	0	0	1	1					
0	1	0	1	1	0	1	0	1					
0	1	1	0	0	0	1	1	1					
0	1	1	0	1	1	0	0	1					
0	1	1	1	0	1	0	1	1					
0	1	1	1	1	1	1	0	1					
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1	0	0	0	1	0	0	1	0					
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1	0	1	0	0	1	0	0	0					
1	0	1	0	1	1	0	1	0					
1	0	1	1	0	1	1	0	0					
1	0	1	1	1	1	1	1	0					
1	1	0	0	0	0	0	0	0					
1	1	0	0	1	0	0	0	1					
1	1	0	1	0	0	0	1	1					
1	1	0	1	1	0	1	0	1					
1	1	1	0	0	0	1	1	1					
1	1	1	0	1	1	0	0	1					
1	1	1	1	0	1	0	1	1					
1	1	1	1	1	1	1	0	1					
1	0	0	0	0	1	1	1	1					

Table 3-6

6. When E=0, circuit operates BCD addition. When E=1, circuit operates BCD subtraction. If C4=1 meaning the result of subtraction is positive, if C4=0 meaning the result of subtraction is negative. Is the addition of input A and B in table 3-6 the same as the experiment?

### 3-4 Questions & discussion

