Chapter 6 Flip-flop Practice

6-1 Practice purpose

1. To understand all flip-flops
2. To understand flip-flops' logic function
3. To understand the switch among flip-flops

6-2 Practice theory

Flip-flop or bisatble contains only two stable circuits which are the basic elements in digital circuits. It also is the basic element of memory, counter,
divider and shift register. It is mainly the storage device of BJT which latches have the same function.

There are many flip-flops but this chapter is about the basic flip-flop, to establish a basic and complete concept.

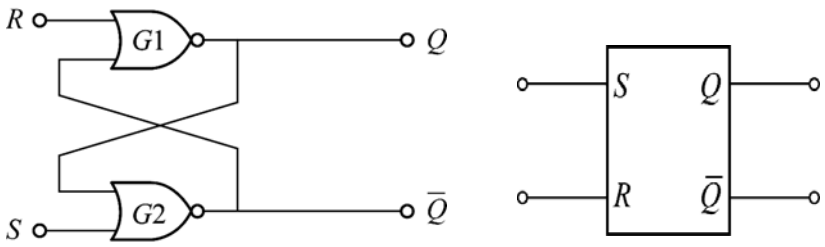
In chapter 5, we have discussed combinational logic and its design process. These logic circuits are all made by basic logic gates; they do not have any memory function and their output states only relate the input states at the processing moment. But in reality, we always hope the device has memory function, which means that the system's output and input relates at the processing time, but also it has to relate to the "state" which is called Sequential circuit. The basic element of Sequential circuit includes all the logic gates which we have mentioned before and also the memory elements. These elements are what we called flip-flops, which are like multi vibrators. Types of flip-flops vary because of the structures. In general, they include SR flip-flop, JK flip-flop, D model flip-flop and T model flip-flop.

6-2-1 SR Flip-flop

1. SR flip-flop made by NOR

We are going to introduce the first flip-flop, SR flip-flop. Figure 6-1(a) is the SR flip-flop made by NOR gate. Figure 6-1(b) is SR flip-flop's logic Figure. In figure 6-1(a), we can see that both NOR gates' outputs go back to another NOR gate's input which gives SR the function of memory. Also, SR flip-flops have R and S's control inputs to control the flip-flop's state. If R=S=0, then the two NOR gates equal two flip-flops. If you analyze this circuit, it is easy see that a flip-flop's output has something to do with its past history which means if Q=1, and input R=S=0, Q still stays 1. To be more specific, if R=S=0, then the whole flip-flop is not affected. If R=1, S=0, then G1 gate output is 0, which has nothing to do with Q's original value and it results in the output as 0 anyway. This 0 value goes back to G2 gate's input and S=0 goes to G2 gates to make Q as 1. Remember that no matter what Q's original value is, the result is always the same. Therefore, we conclude that if R=1, S=0, then Q=0, $\overline{Q}$ = 1. The result is not influenced.

If R=0, S=1, then Q=1, $\overline{Q}$ = 1.



(a) (b)

Figure 6-1 SR flip-flop made by NOT: (a) logic figure (b) logic symbols

When using SR flip-flop, we usually avoid setting both R and S as 1, because the result cannot be predicted as the first three situations might cause unnecessary inaccuracy.

S R	Q $\overline{Q}$
0 0	0 or1 1 or 0
0 1	0 1
1 0	1 0
1 1	Not allowed

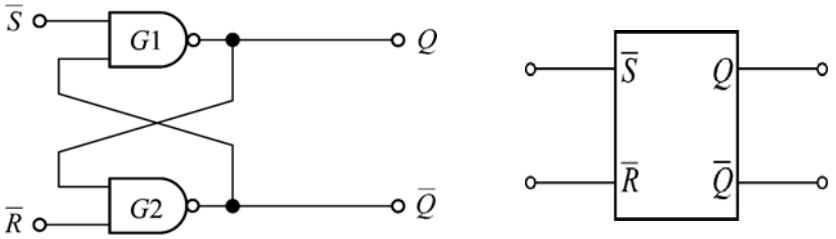
S R	Q_{n+1} $\overline{Q_n}+1$
0 0	Q_n $\overline{Q_n}$
0 1	0 1
1 0	1 0
1 1	Not allowed

Figure 6-2 SR flip-flop's truth table made by NOR

Using the truth table can clearly show SR flip-flop's states. Figure 6-2 is SR flip-flop's truth table.

2. SR flip-flop made by NAND

We know that any NOR made circuits can be remade by NAND and also serve the same function. SR flip-flop is the same. Figure 6-3 is an SR flip-flop made by NAND; its working theory is the same as NOR flip-flop. Figure 6-4 is the truth table of SR flip-flop made by NAND, you can find the supplement relationship between NAND SR flip-flop and NOR SR slip-flop. So we present them with S and R.



(a) (b)

Figure 6-3 NAND gate SR flip-flop (a) logic figure (b) logic symbols

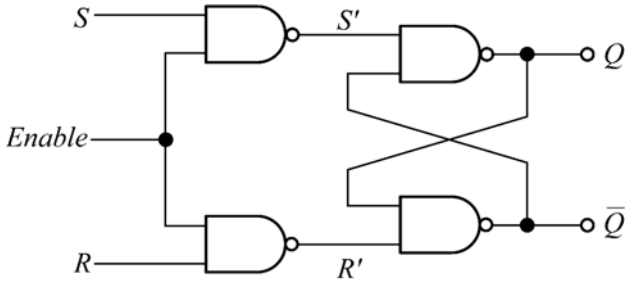
$\overline{S}$ $\overline{R}$	Q $\overline{Q}$
0 0	Not allowed
0 1	1 0
1 0	0 1
1 1	0 or 1 1 or 0

$\overline{S}$ $\overline{R}$	Q_{n+1} $\overline{Q_{n+1}}$
0 0	Not allowed
0 1	1 0
1 0	0 1
1 1	Q_{n+1} $\overline{Q_n}$

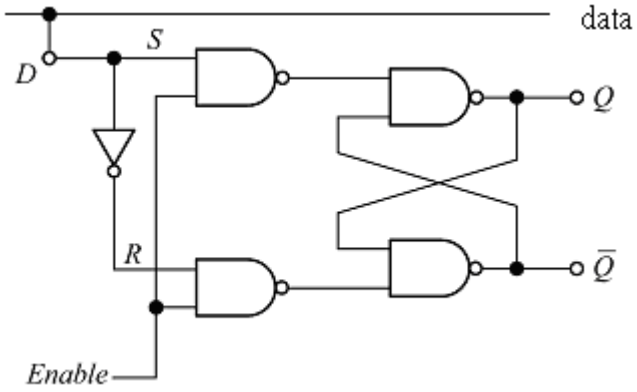
Figure 6-4 Truth table of NAND SR flip-flop

3. SR flip-flop with control ends

SR flip-flop's S and R (or $\overline{S}$ and $\overline{R}$) are called data inputs, because the signals of the two inputs decide which data (0 or 1) is saved in the flip-flop.
In reality, a control device is always needed to be installed, to make SR flip-flop connect to data source or to be isolated. The controlling SR flip-flop is as figure 6-5.



(a)



(b)

Figure 6-5 (a) controlling SR flip-flop (b) controlling D model flip-flop

When Enable=0, G1 and G2 are disabled. The output end is 1, flip-flop and input data isolated. At this point, no matter what S and R's inputs are, $S' = R' = 1$. It means SR flip-

flop's next state decides the past state, which means the flip-flop's state is not changeable. For $S'=R'=1$ working state, please refer to figure 6-4's s truth table. When Enable=1, $S'=\overline{S}$, $R'=\overline{R}$, meanwhile, SR flip-flop is as figure 6-3 which is a NAND gate SR flip-flop. The input signal onto Enable is called gate or strobe. This kind of SR flip-flop is also called dynamic SR flip-flop, which is different from static SR flip-flop.

Figure 6-5(b) is the appliance of dynamic SR flip-flop. We are going to send data line to SR flip-flop's D input end. The data line is from a multiple-line bus and its data sending is changed along the time. On some occasions we hope to get data line's D (0 or 1) to complete this movement. We can use ENABLE to start SR flip-flop. Because S=D and $R=\overline{D}$, refer to figure 6-4 truth table. We get *Q=D,* so as long as ENABLE is working, flip-flop's output Q changes along with input data D. If we want to keep the data, we only have to shut down ENABLE=0. This kind of delete or save single data SR flip-flop is also called D model flip-flop.

Figure 6-6's waveform model is to show D model flip-flop's working status. When the time is $T_{0,}$ flip-flop is shut down. Because G(Enable) is at active low. If we assume that the flip-flop is lower electric potential, which means Q=0, then no matter how D changes, Q is always 0. From t1 to t2, flip-flop starts, then Q changes along with D. When it is T2, flip-flop is shut down, and data D=1 is kept and saved; some other changes are shown during t3 and t4 period.

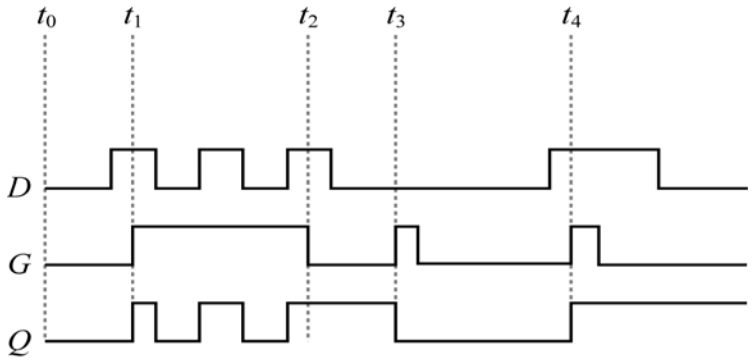
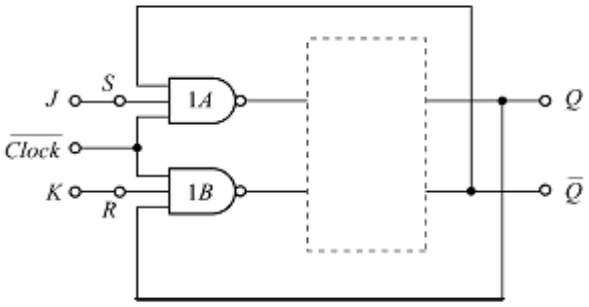


Figure 6-6 D model flip-flop working status' waveform

6-2-2 JK Flip-flop, T Flip-flop

So far, we have avoided setting SR flip-flop's R and S ends 1 at the same time, because under these circumstances we also try to set and reset the flip-flop, but it causes uncertain results. Therefore we hope to improve this fault by making S=R=1 and make it a proper flip-flop.
The improved flip-flop is as figure 6-7. The rectangle where the dotted line is located is the SR flip-flop we talked about earlier and now we have added two more input gates and

it has become an improved flip-flop. The flip-flop's inputs are called J and K instead of S and R. Also the flip-flop is renamed and has become a normal JK flip-flop.
Now it is easier for readers to see the relationship between input, output and state. Its truth table is as figure 6-7(b), Qn means the flip-flop's present state, Qn+1 means the next state. From the truth table we realize that when J=K=0 or J=0, K=1 or J=1, K=1, JK flip-flop's working function is totally the same as SR flip-flop. And when J=K=1, JK flip-flop changes its present state. For example, if Qn=1, then at the next timing period JK flip-flop's state is Qn+1=0; therefore in the figure it is shown as $Q_{n+1}=\overline{Q}_{n}$.



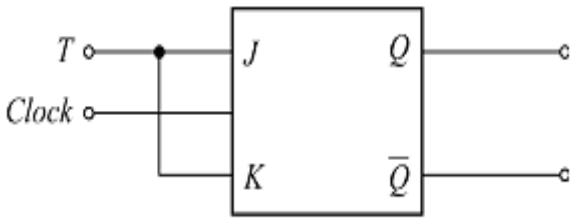
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

(a) **(b)**

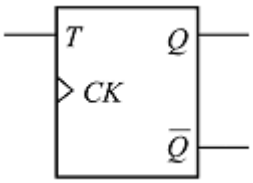
Figure 6-7 (a) JK flip-flop (b) Truth table

If we connect two inputs of JK flip-flop together as figure 6-8, because J=K, that then as long as the input is not 0, when it reaches the stimulating point, the flip-flop will change the state. But if J=K=0, then the stimulating point will not cause flip-flop to change the state, which is because of JK flip-flop's character. When J=K=0, $Q_{n+1}=\overline{Q}_{n}$ and when J=K=1, $Q_{n+1}=\overline{Q}_{n}$. For convenience, we see this flip-flop connecting J and K's JK flip-flop on another model and call it toggle flip-flop or in short, T flip-flop. Its input is T.

So when T=1, T flip-flop changes its state.



(a) JK made T flip-flop



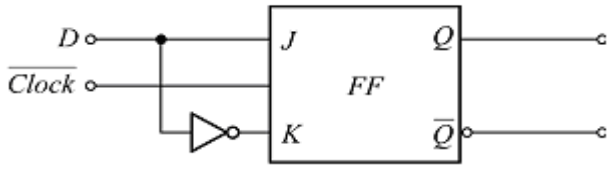
T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

(b) T model flip-flop **(c) Truth table**

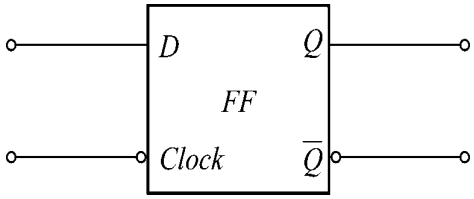
Figure 6-8 T model flip-flop

6-2-3 D flip-flop

In figure 6-5, we mentioned how to change SR latch to D model latch. We also can change SR flip-flop to D flip-flop. So if we connect data line to S end through main and sub flip-flop, at the same time, we connect data line to R end, as figure 6-9, we get D model flip-flop. The logic is as figure 6-9(b).



(a)



D	S R	Q
0	0 1	0
1	1 0	1

(b) **(c)**

Figure 6-9 ((a) SR flip-flop made D flip-flop (b) Logic symbols (c) Truth table

In digital system, we often need to send a series of input data to another part through timing; at this point, D flip-flop is doing this job. As you know, D flip-flop actually sends input data from input end (D) to output end (Q). If D flip-flop is stimulated by the wave and the input data is sent to D end at t1 time, then the flip-flop has to wait for the next timing period $t_1+\Delta t$ to be stimulated, which means input data is then shown at the output end. Therefore, except for the D flip-flop's minor delay, the whole data delivery is actually late because of D flop-flop's extra timing period. This is why we call it D flip-flop, D as data or delay.

It would be easier to understand if we show the above mentioned with wave changes, see figure 6-10.

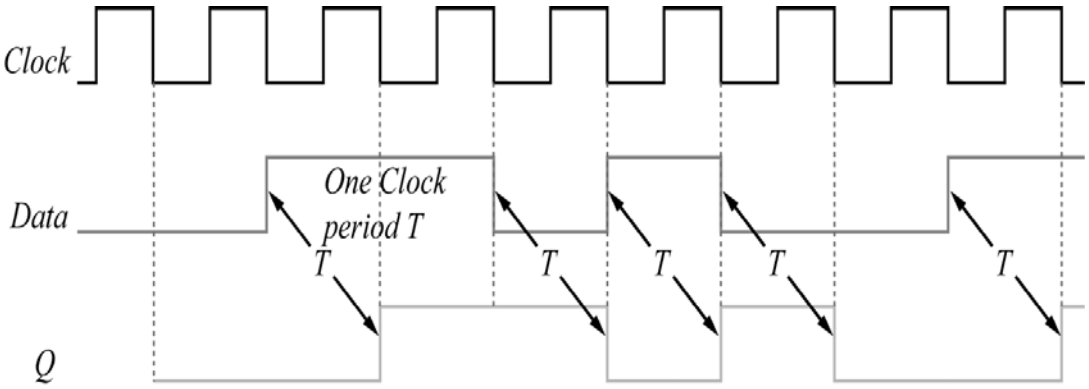


Figure 6-10 D flip-flop sending input data, timing period causes delay but reaches the same effect

In this figure, the triggering edge is the same as data changing time. In fact, the data changing time is a little bit slower than the triggering transition. This "little bit slower" timing has a lot to do with logic gate or other flip-flops' delay. The delay is caused by D flip-flop's previous stage flip-flop which is triggered by the same wave as D flip-flop. Therefore, when the wave triggers the previous stage flip-flop, the output end changes its state because of sending delay, the output end connects D flip-flop's input end. Therefore, D flip-flop's input data change is slower than the trigger wave's change.

6-3 Practice items

Experiment steps

1. 6-3-1 R-S Flip-flop circuit, as figure 6-11.

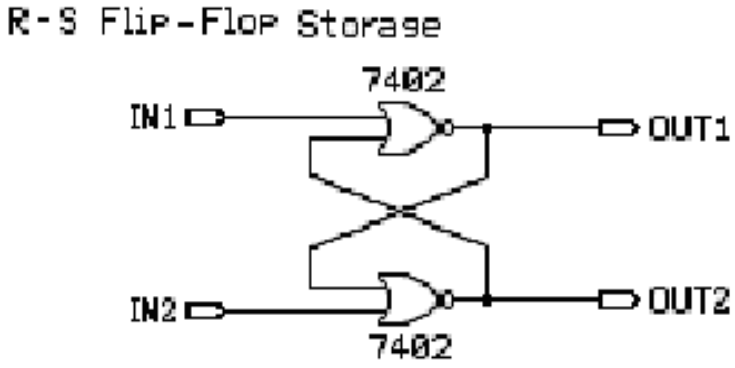


Figure 6-11

2. Input: Connect CON7 S1 to CON1 IN1

Connect CON7 S2 To CON1 IN2

Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1

Connect CON4 OUT2 to LED DISPLAY CON15 Q2

3. Press S1, S2, as table 6-1. 0 means low logic, LED off, 1 means high logic, LED on.

4. Record LED changes in table 6-1.

S(S2)	R(S1)	Q(Q1)	$\overline{Q}$ (Q2)
0	0		
0	1		
1	0		
1	1		

Table 6-1

6-3-2

Experiment steps

1. J-K Flip-flop circuit, as figure 6-12.

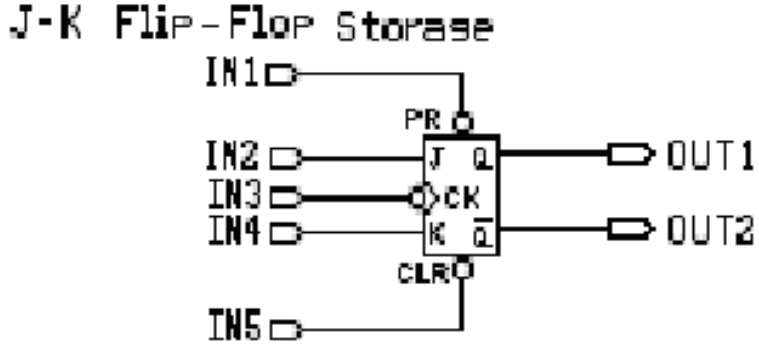


Figure 6-12

2. Input: Connect CON5 CLK 1HZ to CON1 IN1

Connect CON7 S1 toCON1 IN2

Connect CON7 S2 to CON1 IN3

Connect CON7 S3 to CON1 IN4

Connect CON7 S4 to CON1 IN5

Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1

Connect CON4 OUT2 to LED DISPLAY CON15 Q2

3.Switch S1(J), S2(K), S3(PR), S4(CLR) as table 6-2. 0 means low logic, LED off, 1 means high logic, LED on.

4.Record LED changes to table 6-2.

PR	*CLR*	*CK*	*J*	*K*	*Q*(Q1)	$\overline{Q}$ (Q2)
0	1	X	X	X		
1	0	X	X	X		
1	1	1	0	0		
1	1	1	1	0		
1	1	1	0	1		
1	1	1	1	1		

Table 6-2

6-3-3 T Flip-flop

Experiment steps

1. JK flip-flop (T flip-flop) circuit, as figure 6-13.

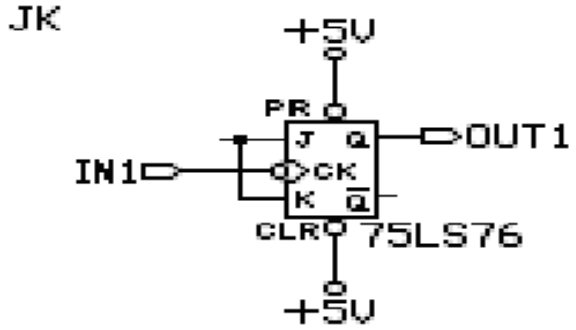


Figure 6-13

2. Input: Connect CON5 CLK 1 HZ to CON1 IN1
Connect CLR and PR to HI
Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1

3. Switch CLOCK input, as table 6-3. 0 means low logic, LED off, 1 means high logic, LED on.

4. Record LED changes in table 6-3.

T	Q	$\overline{Q}$

0		
1		
0		
1		

Table 6-3

6-3-4 D Flip-flop

Experiment steps

1. D flip-flop circuit, as figure 6-14.

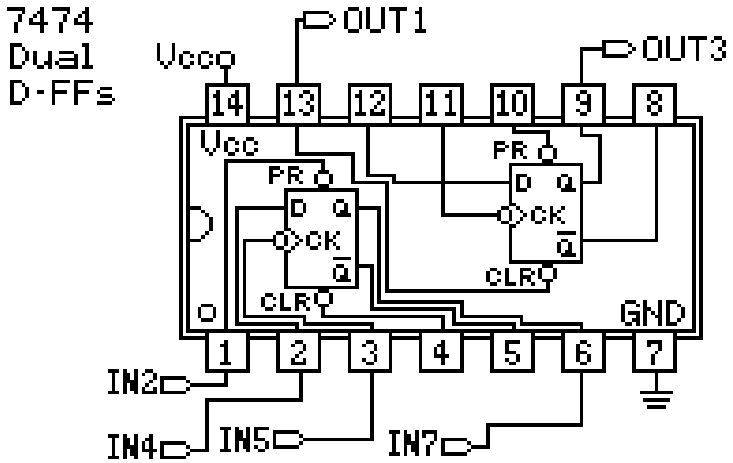


Figure 6-14

2. Input: Connect CON5 CLK 1HZ to CON1 IN1
   Output: Connect CON4 OUT1 to LED DISPLAY CON15 Q1
   Connect CON4 OUT2 to LED DISPLAY CON15 Q2
3. Switch S1, S2, S3, as table 6-4 0 means low logic, LED off, 1 means high logic, LED on.
4. Record LED changes in table 6-4.

PR	CLR	D	CK	Q	$\overline{Q}$
0	1	X	X		
1	0	X	X		
0	0	X	X		
1	1	1	X		
1	1	0	X		

Table 6-4

6-4 Questions & Discussion

1. D flip-flop's $\overline{Q}$ output end connects to D output end. Prove D flip flop changes to T flip flop.
2. There is a small circle on the CLOCK, please explain its meaning.
3. What is the main purpose of a flip-flop?
4. (a) What is the wave frequency of Q_A?
   (b)What is the wave frequency of Q_B?